TESTING FOR THE VERIFICATION OF COMPLIANCE OF PV INVERTER WITH :

AS / NZS 4777.2:2015 GRID CONNECTION OF ENERGY SYSTEMS VIA INVERTERS

(PART 2: INVERTER REQUIREMENTS)

Procedure: PE.T-LE-62

Test Report Number:	**2220-0288**
Trademark:	SOFAR SOLAR
Tested Model:	**HYD 15KTL-3PH**
Variant Models:	**HYD 5KTL-3PH, HYD 6KTL-3PH, HYD 8KTL-3PH, HYD 10KTL-3PH, HYD 20KTL-3PH.**

APPLICANT

Name:	**Shenzhen SOFAR SOLAR Co., Ltd.**
Address:	401, Building 4, AnTongDa Industrial Park, District 68, XingDong Community, XinAn Street, BaoAn District, Shenzhen City, Guangdong Province, P.R. China

TESTING LABORATORY

Name:	**SGS Tecnos, S.A. (Electrical Testing Laboratory)**
Address:	C/ Trespaderne, 29 - Edificio Barajas 1 28042 MADRID (Spain)
Conducted (tested) by:	Michael Tong (Project Engineer)
Approved by:	Jacobo Tevar (Technical Reviewer)
Date of issue:	16/09/2020
Number of pages:	171

SGS Tecnos, S.A.
Laboratorio de Ensayos E&E

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Test Report Historical Revision:

Test Report Version	Date	Resume
2220-0288	16/9/2020	First issuance

INDEX

1 SCOPE

SGS Tecnos, S.A. (Electrical Testing Laboratory) has been contract by Shenzhen SOFAR SOLAR Co., Ltd, in order to perform the testing according the AS/NZS 4777.2: 2015: Grid connection of energy systems via inverters. Part 2: Inverter requirements.

For the purpose of this test report, it is to be used for the certification for Australia only, but further tests having settings for New Zealand (Volt – Watt Response Mode, Frequency trip tests, Volt - watt response mode for charging of energy storage and Sustained operation for voltage variations) have just been included for information purposes.

2 GENERAL INFORMATION

2.1 Testing Period and Climatic conditions

The necessary testing has been performed between the 3rd of June to the 9th of September of 2020.

All the tests and checks have been performed at 25 ± 5ºC, 96 kPa ± 10 kPa and 50% RH ± 10% RH.

SITE TEST

Name...: Shenzhen SOFAR SOLAR Co., Ltd.

Address ....: 401, Building 4, AnTongDa Industrial Park, District 68, XingDong Community, XinAn Street, BaoAn District, Shenzhen City, Guangdong Province, P.R. China

2.2 Equipment under Testing

Apparatus type .... : Hybrid Inverter

Installation .... : Fixed (permanent connection)

Manufacturer .... : Shenzhen SOFAR SOLAR Co., Ltd.

Trade mark .... : SOFAR SOLAR

Model / Type reference .... : HYD 15KTL-3PH

Serial Number .... : SP1ES020H71002

Software Version.. : ARM Software Version: V2.00
MAIN DSP Software Version: D010136
Slave DSP Software Version: D010134

Rated Characteristics.................................. : PV side: 180-960Vdc MPPT, 1000Vdc Maximum, 25A/25A Maximum.
Battery side: 180-800Vdc, 25/25Ad.c. Maximum for both charging and discharging.
AC output: 230/400Vac; 50/60Hz; 21.7Aa.c. Rated (*), 24Aa.c. Maximum; 15000W Rated, 16500VA Maximum.
AC back-up: 230/400Vac, 50/60Hz, 24Aa.c. Maximum, 16500VA Maximum.
(*) The rated output current is calculated using rated voltage and rated power.

Date of manufacturing: 2020

Test item particulars

Input .... : PV, AC and Batteries

Output.. AC

Class of protection against electric shock... : Class I

Degree of protection against moisture .... : IP 65

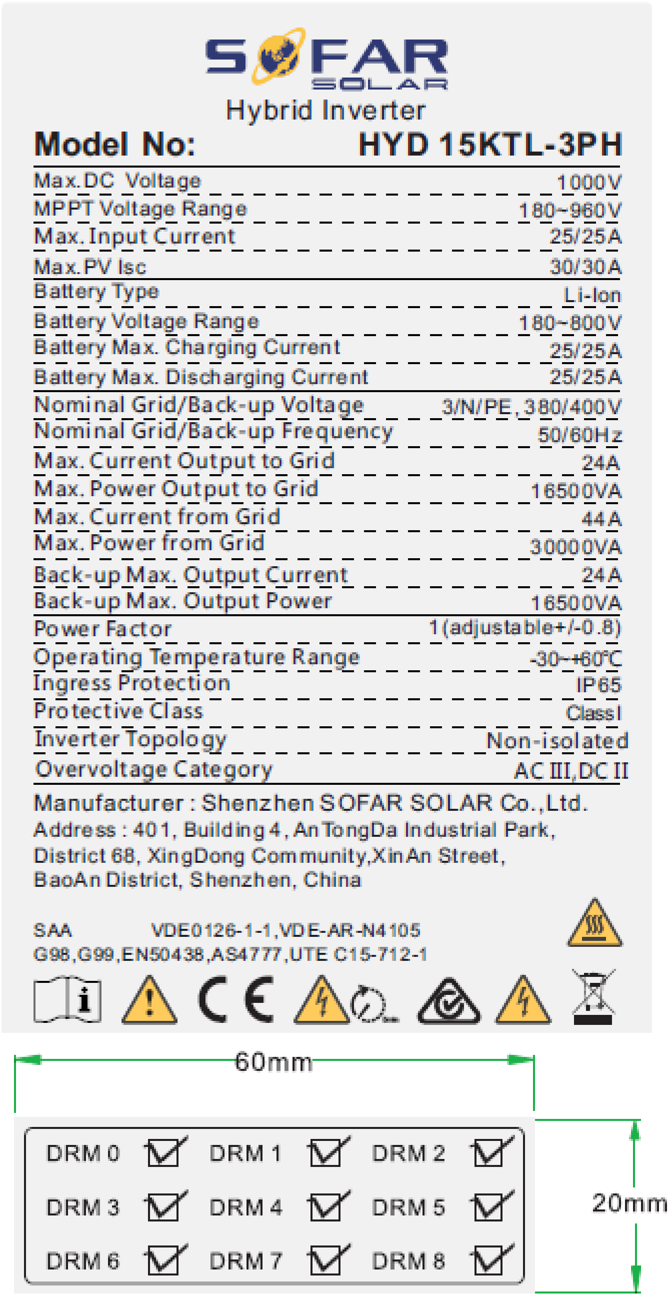
Type of connection to the main supply .... : Three phase – Fixed installation

Cooling group... : Fans:(Model HYD-20KTL-3PH, HYD-15KTL-3PH, HYD-10KTL-3PH); Heatsink:(Model HYD-8KTL-3PH, HYD-6KTL-3PH, HYD-5KTL-3PH)

Modular .... : No

Internal Transformer................................... : No

Copy of rating plate (representative):



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation.
3. Labels of other models are as the same with **HYD 15KTL-3PH**'s except the parameters of rating.

Equipment under testing:

- **HYD 15KTL-3PH**

The variants models are:

- **HYD 5KTL-3PH**
- **HYD 6KTL-3PH**
- **HYD 8KTL-3PH**
- **HYD 10KTL-3PH**
- **HYD 20KTL-3PH**

Model Number	**HYD 5KTL-3PH**	**HYD 6KTL-3PH**	**HYD 8KTL-3PH**	**HYD 10KTL-3PH**	**HYD 15KTL-3PH**	**HYD 20KTL-3PH**
Battery Input Data						
Battery Voltage Range	180V-800V					
Battery Voltage Range for full load	200V~800V	240V~800V	320V~800V	200V~800V	300V~800V	400V~800V
Nominal charging/discharging Power	10000W	15000W	20000W	10000W	15000W	20000W
Max. charging/discharging Current	25A			50A(25A/25A)		
PV Input Data						
Max. DC Voltage	1000V					
MPPT Voltage Range	180-960Vd.c.					
Full power MPPT Voltage Range	250V~850V	320V~850V	360V~850V	220V~850V	350V~850V	450V~850V
Max. Input Current	12.5A/12.5 A	12.5A/12.5 A	12.5A/12.5 A	25A/25A	25A/25A	25A/25A
Max. Short Current	15A/15A	15A/15A	15A/15A	30A/30A	30A/30A	30A/30A
AC Output Data (On-grid)						
Max. AC Output Current	8Aa.c.	10Aa.c.	13Aa.c.	16Aa.c.	24Aa.c.	32Aa.c.
Nominal Grid Voltage	3/N/PE, 230/400Vac					
Nominal Grid Frequency	50Hz					
AC Output Rated Power	5000W	6000W	8000W	10000W	15000W	20000W
Max AC Output Power	5500VA	6600VA	8800VA	11000VA	16500VA	22000VA
Power Factor	0.8 leading to 0.8 lagging					
AC Output Data (Back-up)						
Nominal Output Power	5000W	6000W	8000W	10000W	15000W	20000W
Max. Output Power	5500VA	6600VA	8800VA	11000VA	16500VA	22000VA
Max. Output Current	8A	10A	13A	16A	24A	32A
Nominal Grid Voltage	3/N/PE, 230/400Vac					
Nominal Grid Frequency	50Hz					
General Data						
Ambient Temperature	-30℃~60℃					
Ingress Protection	IP65					
Protective Class	Class I					

The variants models have been included in this test report without tests because the following features don´t change regarding to the tested model:

- Same connection system and hardware topology
- Same control algorithm.
- Output power within 1/√10 and 2 times of the rated output power or the EUT or Modular inverters.
- Same Firmware Version.

The values presented in the following table have been used for calculation of referenced values (p.u.; %) thougth the report if not otherwise indicated.

<table>
<tr><th colspan="2">Reference Values</th></tr>
<tr><td>Rated power, Pn in W</td><td>15000</td></tr>
<tr><td>Rated apparent power, Sn in VA</td><td>15000</td></tr>
<tr><td>Maximum apparent power, Smax in VA</td><td>16500</td></tr>
<tr><td>Rated wind speed (only WT), vn in m/s</td><td>N/A</td></tr>
<tr><td>Rated current (determined), In in A</td><td>21.7</td></tr>
<tr><td>Rated output voltage, (phase to phase) Un in Vac</td><td>230</td></tr>
<tr><td colspan="2">Note: In this report p.u. values are calculated as follows:
-For Active & Reactive Power p.u. values, are referenced to Pn.
-For Currents p.u. values, the reference is always In.
-For Voltages p.u. values, the reference is always Un.</td></tr>
</table>

The results obtained apply only to the particular sample tested that is the subject of the present test report. The most unfavorable result values of the verifications and tests performed are contained herein.

Throughout this report a point (~~comma~~) is used as the decimal separator.

2.3 Test equipment list

From	No.	Equipment Name	Model No.	Equipment No.	Calibration Date	Equipment calibration due date
Sofarsolar	1	Power analyzer	ZLG/PA5000H	C820290908 2002110001	2020/03/02	2021/03/01
	2	Power analyzer	ZLG/PA3000	PA3004-P0004-1422	2020/01/14	2021/01/13
	3	Voltage probe	SanHua / SI-9110	152627	2020/01/14	2021/01/13
	4	Voltage probe	SanHua / SI-9110	111134	2020/01/14	2021/01/13
	5	Voltage probe	SanHua / SI-9110	111152	2020/01/14	2021/01/13
	6	Current probe	CYBERTEK / CP1000A	C181000922	2020/01/14	2021/01/13
	7	Current probe	CYBERTEK / CP1000A	C181000925	2020/01/14	2021/01/13
	8	Current probe	CYBERTEK / CP1000A	C181000929	2020/01/14	2021/01/13
	9	Oscilloscope	KEYSIGHT / DS0X3014A	MY58101647	2020/01/14	2021/01/13
	10	Temperature & Humidity meter	Anymeters / TH101B	ZB-WSDJ-001	2020/01/14	2021/01/13
SGS	11	True RMS Multimeter	Fluke / 187	GZE012-8	2019/12/05	2020/12/04

Note: all measurement equipment was used inside their corresponding calibration period. Copy of all calibration certificates are available at the laboratory for reference.

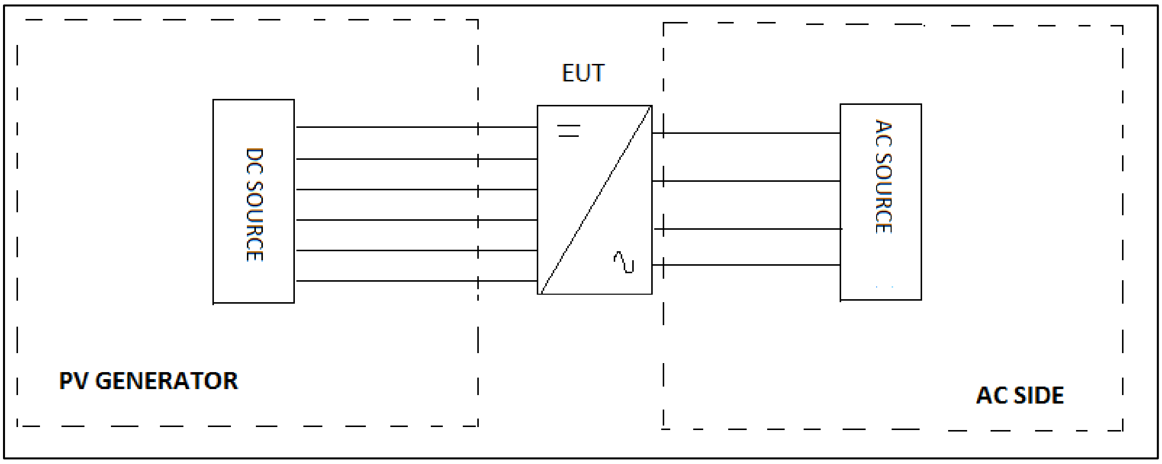
2.4 Measurement uncertainty

Associated uncertainties through measurements showed in this this report are the maximum allowable uncertainties.

Magnitude	Uncertainty
Voltage measurement	±1.5 %
Current measurement	±2.0 %
Frequency measurement	±0.2 %
Time measurement	±0.2 %
Power measurement	±2.5 %
Phase Angle	±1º
Temperature	±3º C
Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the solicitant. Note2: Where the standard requires lower uncertainties that those in this table. Most restrictive uncertainty has been considered.	

2.5 Test set up of the different standard

Below is the simplified construction of the test set up.



Tests requiring batteries were performed using a DC source simulating the behaviour of the battery.

Different equipment has been used to take measures as it shows in chapter 2.3. Current and voltage clamps have been connected to the inverter input/output for all the tests.

All the tests described in the following pages have used this specified test setup.

The test bench used includes:

EQUIPMENT	MARK / MODEL	RATED CHARACTERISTICS	OWNER / ID.CODE
AC source	Kwell / AFG-S-33800	Voltage: 0-600 V 750KVA	Sofarsolar / EP-026
PV source	Kwell / TVS-630kW	Voltage: 0 - 1000 V 630kW	Sofarsolar / EP-027

2.6 Definitions

EUT	Equipment Under Testing	Hz	Hertz
A	Ampere	V	Volt
VAr	Volt-Ampere reactive	W	Watt
Un	Nominal Voltage	In	Nominal current
Pn	Nominal Active Power	Sn	Nominal Apparent Power
Qn	Nominal Reactive Power	p.u	Per unit
V1+	Voltage Positive Sequence	I1+	Current Positive Sequence
V1-	Voltage Negative Sequence	I1-	Current Negative Sequence
Uv	Voltage Imbalance	Ui	Current Imbalance
DRM	Demand Response Mode	THD	Total Harmonic Distortion
I_h	Harmonic Current	U_h	Harmonic Voltage
PST	Severity of Flicker Short-Term	PLT	Severity of Flicker Long-Term
dc	Maximum Variation of Voltage	d(t)	Variation of Voltage
DRED	Demand Response Enabling Device	d max	Maximum Absolute Value of Voltage Variation

3 RESUME OF TEST RESULTS

INTERPRETATION KEYS

Test object does meet the requirement ....: **P** Pass

Test object does not meet the requirement................: **F** Fails

Test case does not apply to the test object ....: **N/A** Not applicable

To make a reference to a table or an annex. ....: See additional sheet

To indicate that the test has not been realized ....: **N/R** Not realized

STANDARD SECTION	STANDARD REQUIREMENTS AS/NZS 4777.2:2015	RESULT
A.5	**Reference network impedance**	**P**
	Network impedance	P
5	**General Requirements**	**P**
5.1	Electrical safety	N/R (*)
5.2	Provision for External Connections	P
5.3	PV Array earth fault/earth leakage detection	N/R (*)
5.4	Compatibility with electrical installation	P
5.5	Power Factor	P
5.6	Harmonics	--
--	Harmonics Current	P
--	Harmonics Voltage	P
5.7	Flickers	P
5.8	Transient voltage limits	P
5.9	DC Current Injection	P
5.10	Current Balance for Three-phase inverters	P
6	**Operational modes and Multiple mode inverters**	**P**
6.2	Inverter Demand Response Modes (DRMs)	P
6.2.1	General	P
6.2.2	Interaction with Demand Response Enabling Device (DRED)	P
6.3	Inverter Power quality response modes	P
6.3.2	Volt response modes	P
6.3.2.2	Volt-Watt response mode	P
6.3.2.3	Volt-Var response mode	P
6.3.2.4	Voltage balanced modes	P
6.3.3	Fixed power factor mode and reactive power mode	P
6.3.4	Characteristics power factor curve for cos ϕ (P) (Power response)	P
6.3.5	Power rate limit	P
6.3.5.3.3	Changes in a.c. operation and control	P
6.3.5.3.4	Changes in energy source operation	P
6.4	Multiple mode inverter operation	P
6.4.2	Sinusoidal output in stand-alone mode (Harmonics voltage)	P
6.4.3	Volt-Watt response mode for charging of energy storage	P
6.5	Security	P
7	**Protective functions for connection to electrical installations and the grid**	**P**
7.2	Automatic disconnection device	P
7.3	Active Anti-Islanding protection	P
7.4	Voltage and frequency limits (passive anti-islanding protection)	P
7.5	Limits for sustained operation.	P
7.5.2	Sustained operation for voltage variations	P
7.5.3	Sustained operation for frequency variations	P
7.5.3.1	Response to an increase in frequency	P
--	Response to a decrease in frequency	P
7.5.3.2	Response to a decrease in grid frequency with energy storage	P

STANDARD SECTION	STANDARD REQUIREMENTS AS/NZS 4777.2:2015	RESULT
7.6	Disconnection on external signal	P
7.7	Connection and reconnection procedure	P
7.8	Security of protection settings	P
8	**Multiple inverter combination**	**N/A**
8.2	Inverter current balance across multiple phases	N/A
8.3	Grid Disconnection	N/A
8.4	Grid Connection and Reconnection	N/A
8.5.1	Single-phase combinations	N/A
8.5.2	Single-phase inverters used in three-phase combinations	N/A
8.5.3	Required Tests for Multiple Inverter Combination	N/A
8.5.4	Multiple Inverters with one Automatic Disconnection Device	N/A
9	**Inverter marking and documentation**	**P**

(*) The compliances with these requirements are stated in the following test reports:

- IEC 62109-1 and IEC 62109-2: test report nº BL-DG2060127-B01 and BL-DG2060127-B01 attachment 1 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.
- IEC 62040-1: test report nº BL-DG2060127-B02 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.

Note: The declaration of conformity has been evaluated taking into account the IEC Guide 115.

4 TEST RESULTS

4.1 REFERENCE NETWORK IMPEDANCE

The network reference impedance used during the tests has been of:

R_A = 0.15 Ohms; X_A = j 0.15 Ohms at 50 Hz;
R_N = 0.10 Ohms; X_N = j 0.10 Ohms at 50 Hz.

4.2 ELECTRICAL SAFETY

As required per the Clause 5.1 of the standard, inverters for use in energy systems with photovoltaic (PV) arrays, the inverters shall comply with the appropriate electrical safety requirements.

The compliances with these requirements are stated in the following test reports:

- IEC 62109-1 and IEC 62109-2: test report nº BL-DG2060127-B01 and BL-DG2060127-B01 attachment 1 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.
- IEC 62040-1: test report nº BL-DG2060127-B02 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.

4.3 PROVISION FOR EXTERNAL CONNECTIONS

The inverter complies with the requirements according to Clause 5.2 of the standard.

4.4 PV ARRAY EARTH FAULT / EARTH LEAKAGE DETECTION

The compliances with these requirements are stated in the following test reports:

- IEC 62109-1 and IEC 62109-2: test report nº BL-DG2060127-B01 and BL-DG2060127-B01 attachment 1 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.

4.5 COMPATIBILITY WITH ELECTRICAL INSTALLATION

According to the requirements stated in the clause 5.4 of the standard, it has been verified that the inverter is able to operate with AC voltage and frequency limits specified in AS 60038 (for Australia).

The inverter shall stay connected providing the maximum of its available active power working in abnormal voltage and/or frequency conditions.

The following tables show the results of the tests performed:

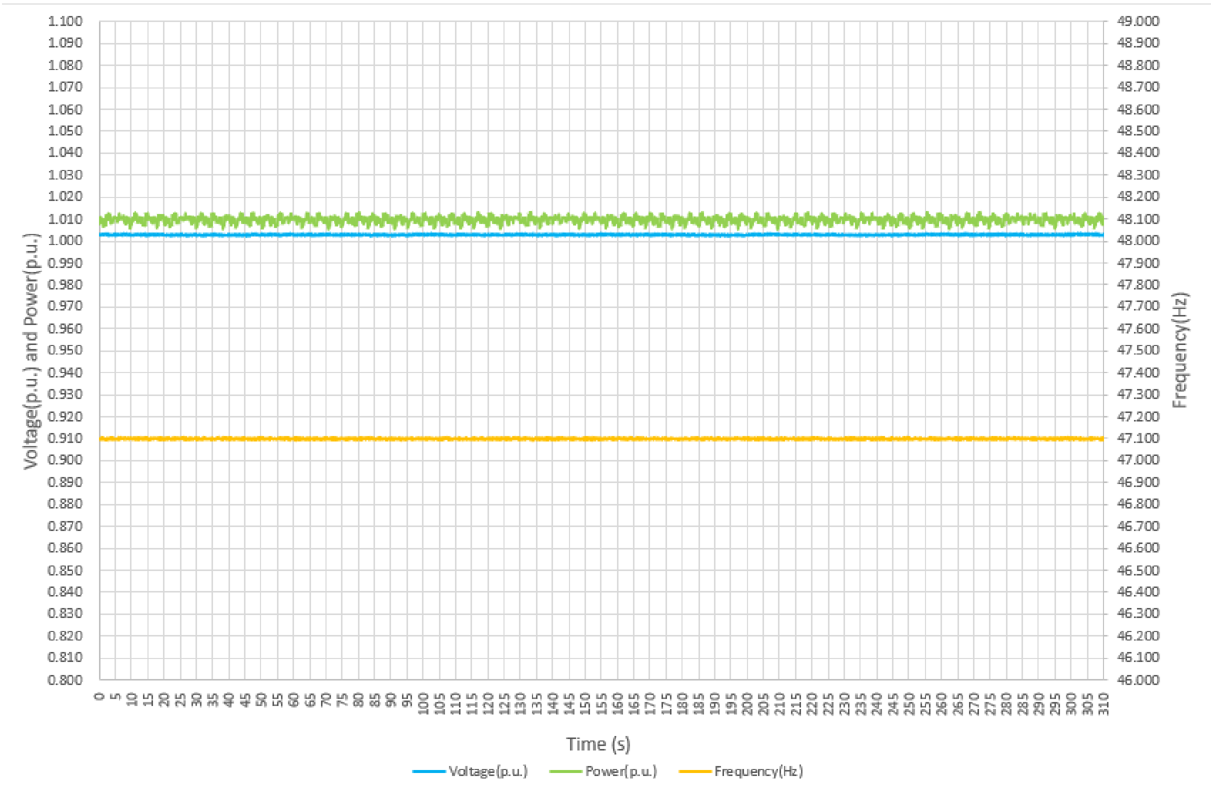
Test 1		Under Frequency		
Voltage	**Frequency**	**Active Power measured**	**Minimum Operation Time**	**Time measured**
100%Un	**47.1Hz**	101.0%Pn	Continuous Operation	> 5 min
Disconnection		☒ NO ☐ YES		

Test 2		Under Voltage		
Voltage	**Frequency**	**Active Power measured**	**Minimum Operation Time**	**Time measured**
94%Un	**50.0Hz**	101.3%Pn	Continuous Operation	> 5 min
Disconnection		☒ NO ☐ YES		

Test 3		Over Voltage + Over Frequency		
Voltage	**Frequency**	**Active Power measured**	**Minimum Operation Time**	**Time measured**
110%Un	**50.25Hz**	100.6%Pn	Continuous Operation	> 5 min
Disconnection		☒ NO ☐ YES		

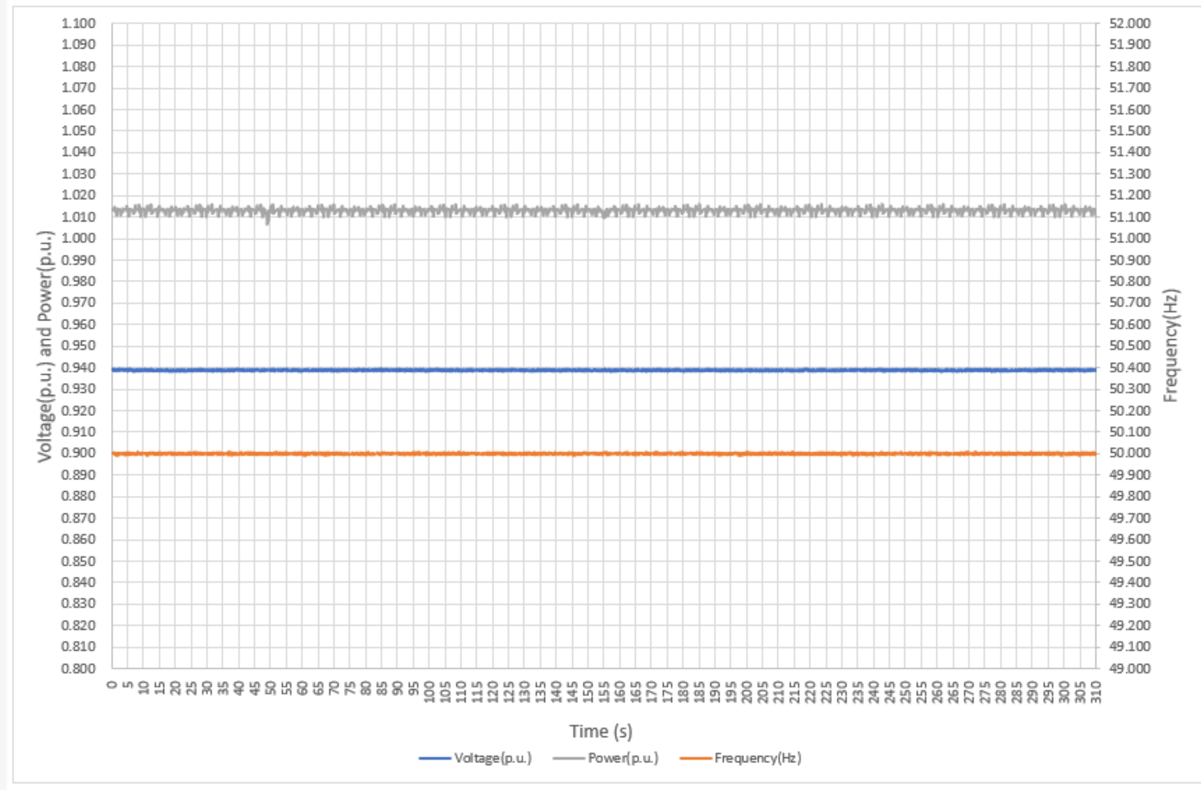
Note: The measured value of active power is calculated as the average of the samples taken each 200 ms during the corresponding measured time.

Test 1 (V = 100%Un and F = 47.1 Hz)	



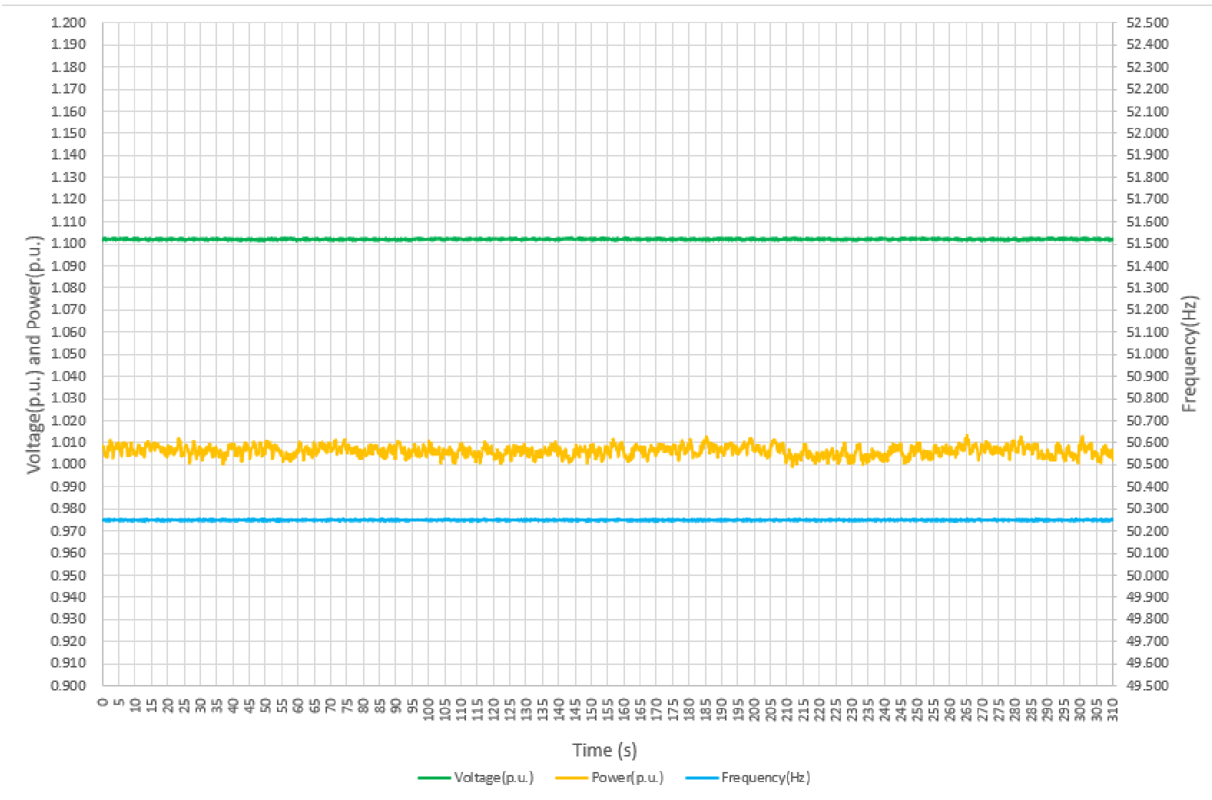
	Time measured: >5 min
Voltage average measured: 100.3 %Un	Frequency measured: 47.10 Hz

Test 2 (V = 94%Un and F = 50.0 Hz)	



	Time measured: >5 min
Voltage average measured: 93.9 %Un	Frequency measured: 50.00 Hz

Test 3 (V = 110%Un and F = 50.25 Hz)



	Time measured: >5 min
Voltage average measured: 110.2 %Un	Frequency measured: 50.25 Hz

4.6 POWER FACTOR

The power factor has been measured according to Clause 5.5 and the annex B of the standard, with an initial power factor at unity.

As the inverter is capable of different power factor settings, the test has been repeated varying the power factor within the range 0.8 leading to 0.8 (*) lagging.

(*) 0.8 leading to 0.8 lagging is more restrictive than 0.95 as the standard required. Refer to point 4.13.2.2 for test results.

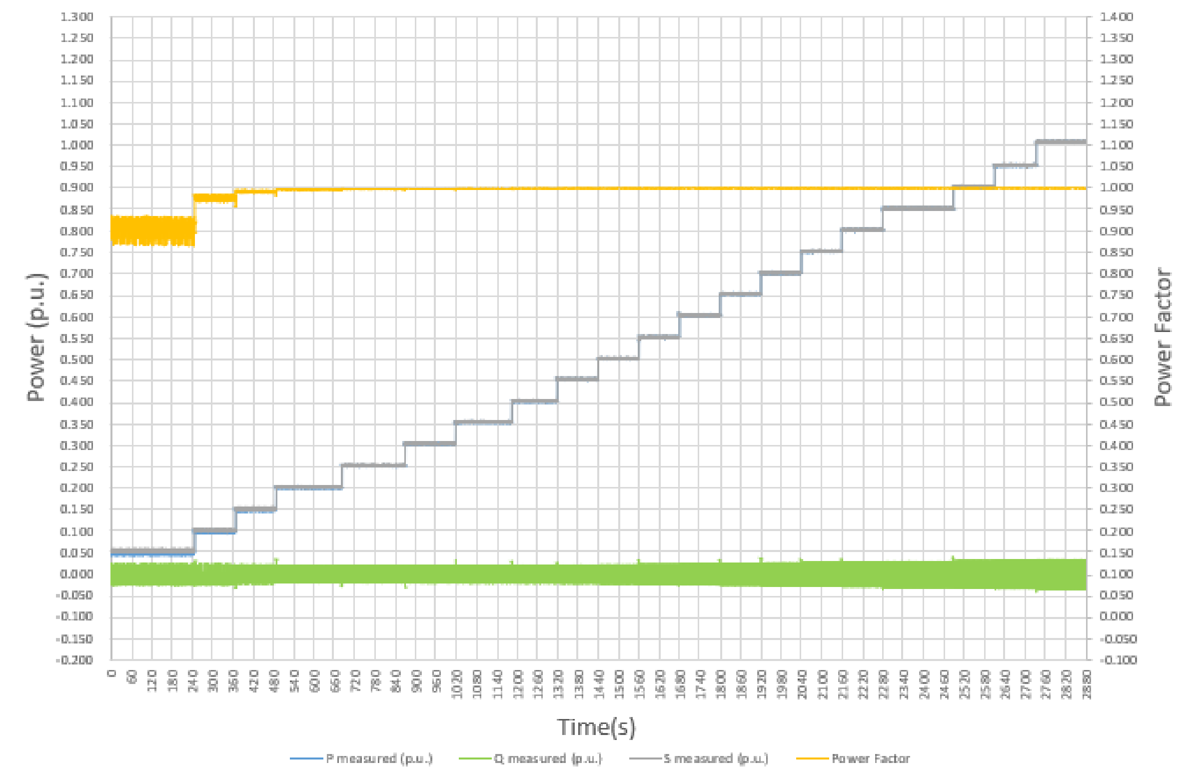
The maximum tolerance allowed for the measured Power Factor is ± 0.01, for measurements from 25%Sn.

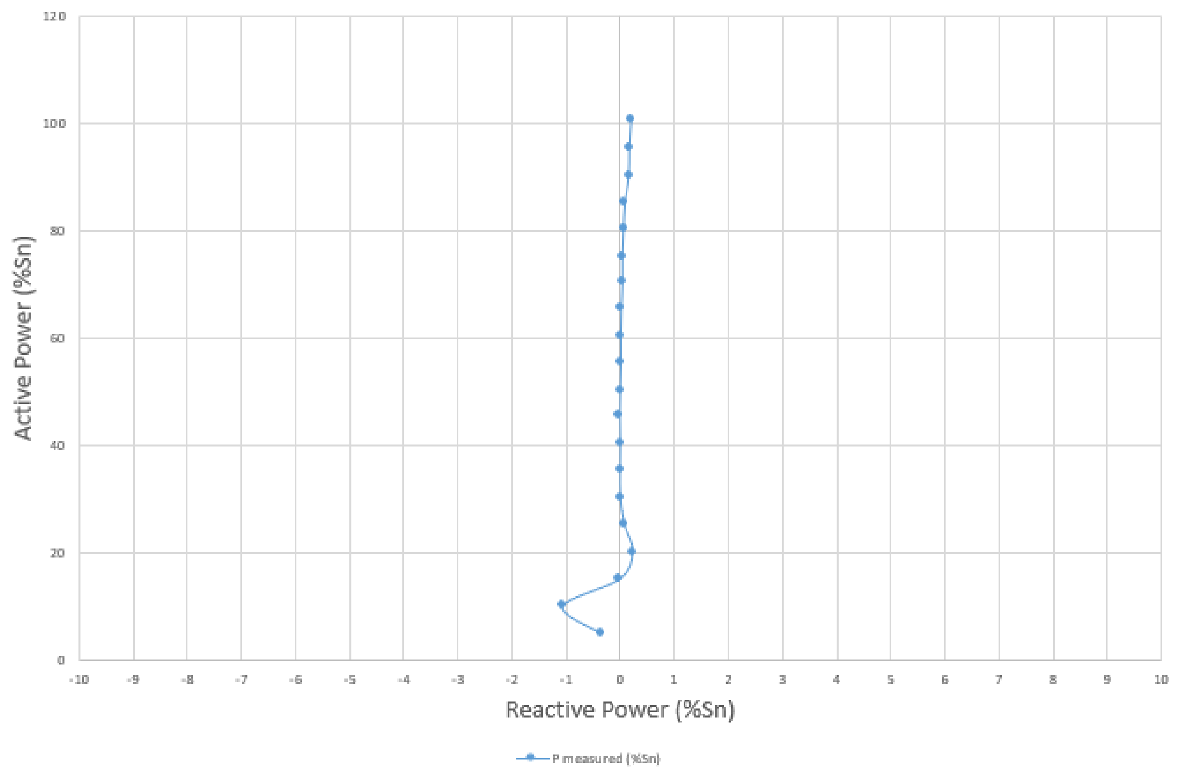
The following table and graphs show test results for measurements of power factor set to unity (PF=1):

Unity Power Factor (PF=1.0)					
P Desired (%Sn)	**P measured (%Sn)**	**Q measured (%Sn)**	**Power Factor Measured (cos φ)**	**Power Factor Desired (cos φ)**	**Power Factor Deviation (cos φ)**
5	4.9	-0.3	0.914	1.000	-0.086 (*)
10	10.0	-1.1	0.980	1.000	-0.020 (*)
15	15.1	0.0	0.992	1.000	-0.008
20	20.2	0.2	0.996	1.000	-0.004
25	25.3	0.1	0.997	1.000	-0.003
30	30.4	0.0	0.998	1.000	-0.002
35	35.4	0.0	0.998	1.000	-0.002
40	40.3	0.0	0.999	1.000	-0.001
45	45.4	0.0	0.999	1.000	-0.001
50	50.3	0.0	0.999	1.000	-0.001
55	55.2	0.0	0.999	1.000	-0.001
60	60.3	0.0	0.999	1.000	-0.001
65	65.3	0.0	0.999	1.000	-0.001
70	70.2	0.1	0.999	1.000	-0.001
75	75.2	0.1	0.999	1.000	-0.001
80	80.3	0.1	0.999	1.000	-0.001
85	85.2	0.1	1.000	1.000	+0.000
90	90.2	0.2	1.000	1.000	+0.000
95	95.2	0.2	1.000	1.000	+0.000
100	100.7	0.2	1.000	1.000	+0.000

(*) It is allowed that the maximum tolerance for the measured Power Factor is outside ± 0.01, for measurements below 25%Sn.

Unity Power Factor (PF=1.0)





4.7 VOLTAGE QUALITY MEASUREMENTS

4.7.1 Current harmonics

The current harmonics have been measured according to the Clause 5.6 of the standard, at the required power values.

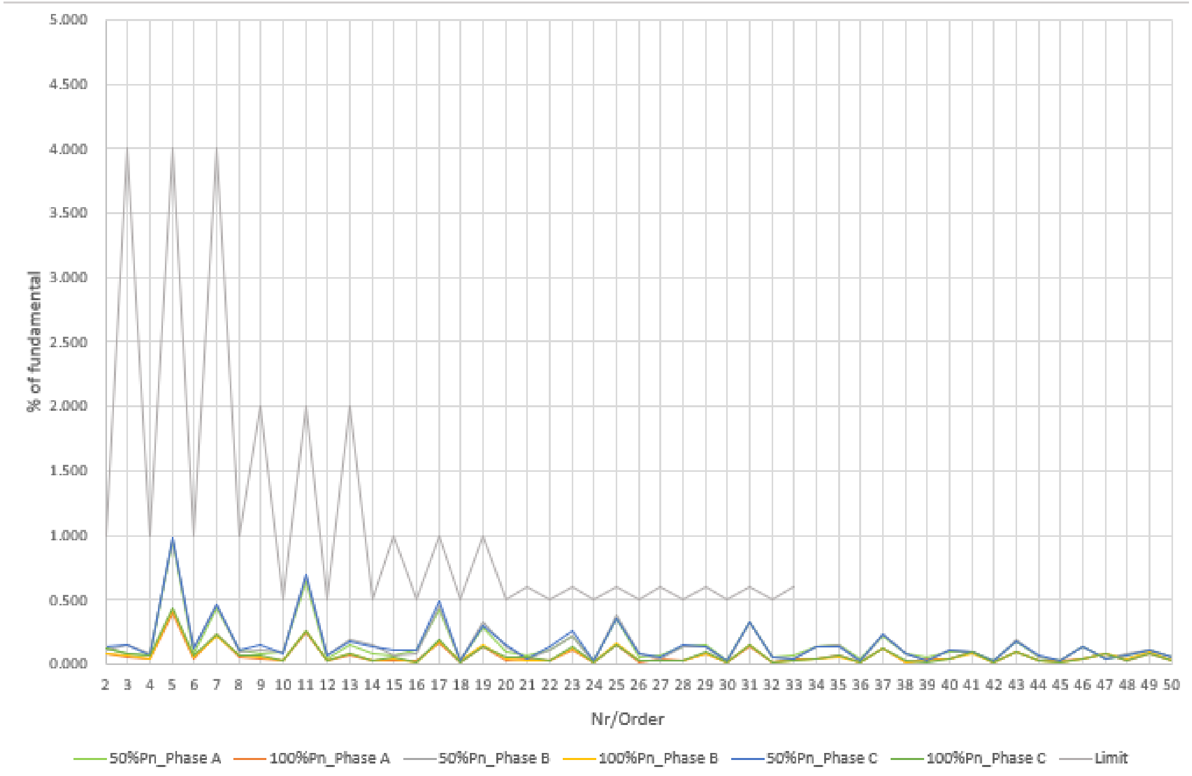
	Limit	50% of rated current (Phase A)	50% of rated current (Phase B)	50% of rated current (Phase C)
Eliminate order	**% of fundamental**	**% of fundamental**	**% of fundamental**	**% of fundamental**
2	1.000	0.128	0.113	0.131
3	4.000	0.077	0.146	0.155
4	1.000	0.073	0.077	0.063
5	4.000	0.955	0.968	0.978
6	1.000	0.085	0.126	0.124
7	4.000	0.438	0.457	0.457
8	1.000	0.114	0.101	0.104
9	2.000	0.078	0.112	0.143
10	0.500	0.093	0.092	0.082
11	2.000	0.634	0.675	0.698
12	0.500	0.047	0.069	0.068
13	2.000	0.150	0.187	0.180
14	0.500	0.082	0.150	0.136
15	1.000	0.074	0.063	0.115
16	0.500	0.108	0.088	0.115
17	1.000	0.418	0.448	0.497
18	0.500	0.027	0.024	0.029
19	1.000	0.293	0.332	0.300
20	0.500	0.094	0.141	0.155
21	0.600	0.061	0.045	0.046
22	0.500	0.114	0.111	0.134
23	0.600	0.222	0.217	0.254
24	0.500	0.026	0.018	0.026
25	0.600	0.351	0.378	0.358
26	0.500	0.056	0.083	0.082
27	0.600	0.068	0.044	0.048
28	0.500	0.132	0.135	0.147
29	0.600	0.146	0.133	0.141
30	0.500	0.034	0.018	0.030
31	0.600	0.321	0.330	0.329
32	0.500	0.050	0.052	0.061
33	0.600	0.067	0.037	0.042
34	--	0.131	0.131	0.140
35	--	0.154	0.148	0.143
36	--	0.038	0.015	0.026
37	--	0.215	0.226	0.230
38	--	0.087	0.076	0.082
39	--	0.051	0.025	0.028
40	--	0.097	0.108	0.110
41	--	0.099	0.100	0.090
42	--	0.021	0.016	0.020
43	--	0.177	0.186	0.171
44	--	0.058	0.059	0.062
45	--	0.028	0.022	0.025
46	--	0.133	0.133	0.138
47	--	0.042	0.045	0.046

	Limit	50% of rated current (Phase A)	50% of rated current (Phase B)	50% of rated current (Phase C)
Eliminate order	% of fundamental	% of fundamental	% of fundamental	% of fundamental
48	--	0.065	0.077	0.070
49	--	0.103	0.106	0.104
50	--	0.054	0.053	0.051
THD	5.000	1.556	1.628	1.663

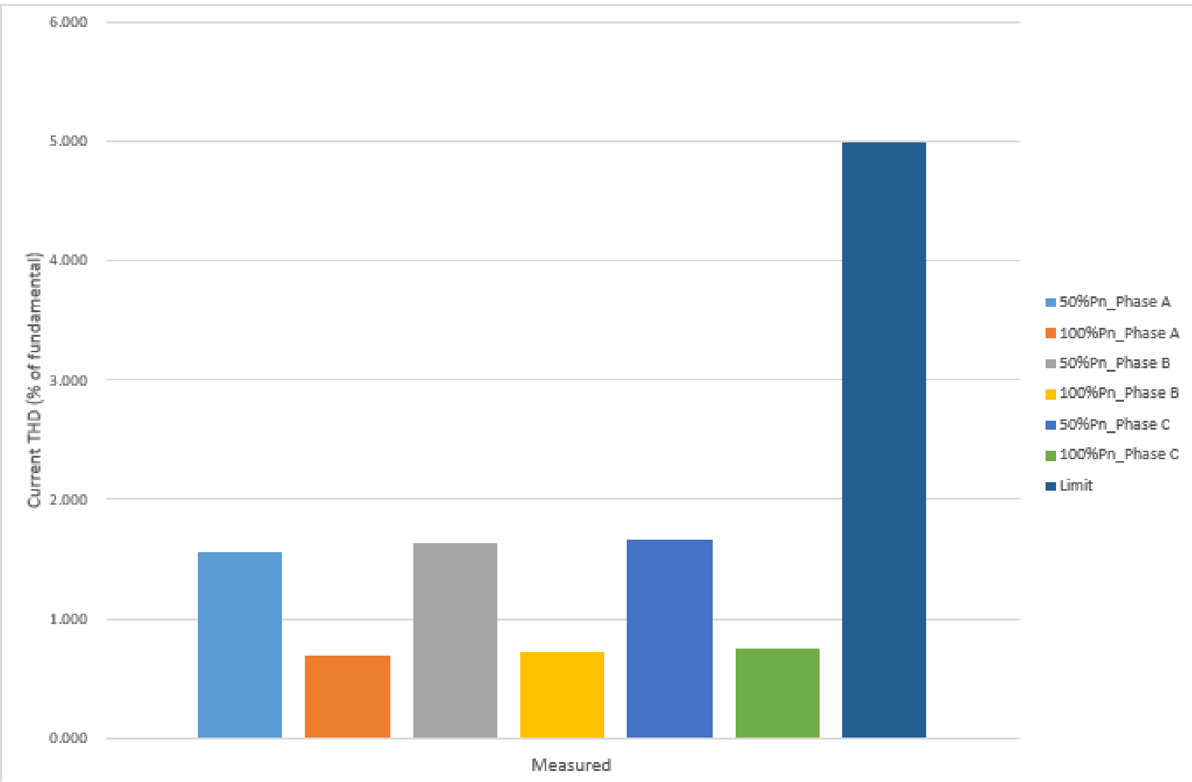
	Limit	100% of rated current (Phase A)	100% of rated current (Phase B)	100% of rated current (Phase C)
Eliminate order	% of fundamental	% of fundamental	% of fundamental	% of fundamental
2	1.000	0.089	0.088	0.126
3	4.000	0.048	0.063	0.087
4	1.000	0.047	0.044	0.067
5	4.000	0.400	0.426	0.431
6	1.000	0.040	0.060	0.067
7	4.000	0.230	0.214	0.230
8	1.000	0.048	0.066	0.070
9	2.000	0.041	0.049	0.065
10	0.500	0.033	0.028	0.030
11	2.000	0.241	0.256	0.264
12	0.500	0.024	0.028	0.025
13	2.000	0.074	0.083	0.089
14	0.500	0.021	0.032	0.023
15	1.000	0.029	0.041	0.051
16	0.500	0.021	0.015	0.018
17	1.000	0.168	0.180	0.196
18	0.500	0.016	0.021	0.017
19	1.000	0.135	0.147	0.137
20	0.500	0.033	0.038	0.053
21	0.600	0.037	0.032	0.049
22	0.500	0.025	0.022	0.024
23	0.600	0.109	0.120	0.132
24	0.500	0.012	0.014	0.013
25	0.600	0.154	0.161	0.155
26	0.500	0.016	0.027	0.025
27	0.600	0.041	0.031	0.032
28	0.500	0.032	0.031	0.031
29	0.600	0.082	0.082	0.095
30	0.500	0.011	0.010	0.010
31	0.600	0.142	0.148	0.145
32	0.500	0.012	0.016	0.018
33	0.600	0.038	0.024	0.021
34	--	0.037	0.038	0.037
35	--	0.064	0.057	0.070
36	--	0.012	0.009	0.009
37	--	0.124	0.128	0.129
38	--	0.019	0.019	0.024
39	--	0.036	0.023	0.014
40	--	0.037	0.038	0.038
41	--	0.091	0.076	0.090
42	--	0.011	0.009	0.009
43	--	0.089	0.100	0.099
44	--	0.030	0.026	0.030
45	--	0.026	0.017	0.014

	Limit	100% of rated current (Phase A)	100% of rated current (Phase B)	100% of rated current (Phase C)
Eliminate order	**% of fundamental**	**% of fundamental**	**% of fundamental**	**% of fundamental**
46	--	0.041	0.046	0.042
47	--	0.085	0.076	0.082
48	--	0.030	0.035	0.031
49	--	0.087	0.091	0.087
50	--	0.025	0.023	0.025
THD	5.000	0.688	0.718	0.750

Current Harmonics



THD



4.7.2 Voltage harmonics

The background voltage harmonics have been verified according to the Clause 5.6 (Appendix C) of the standard, into AC terminals of the grid source.

The test results are shown in the graphic and the table below.

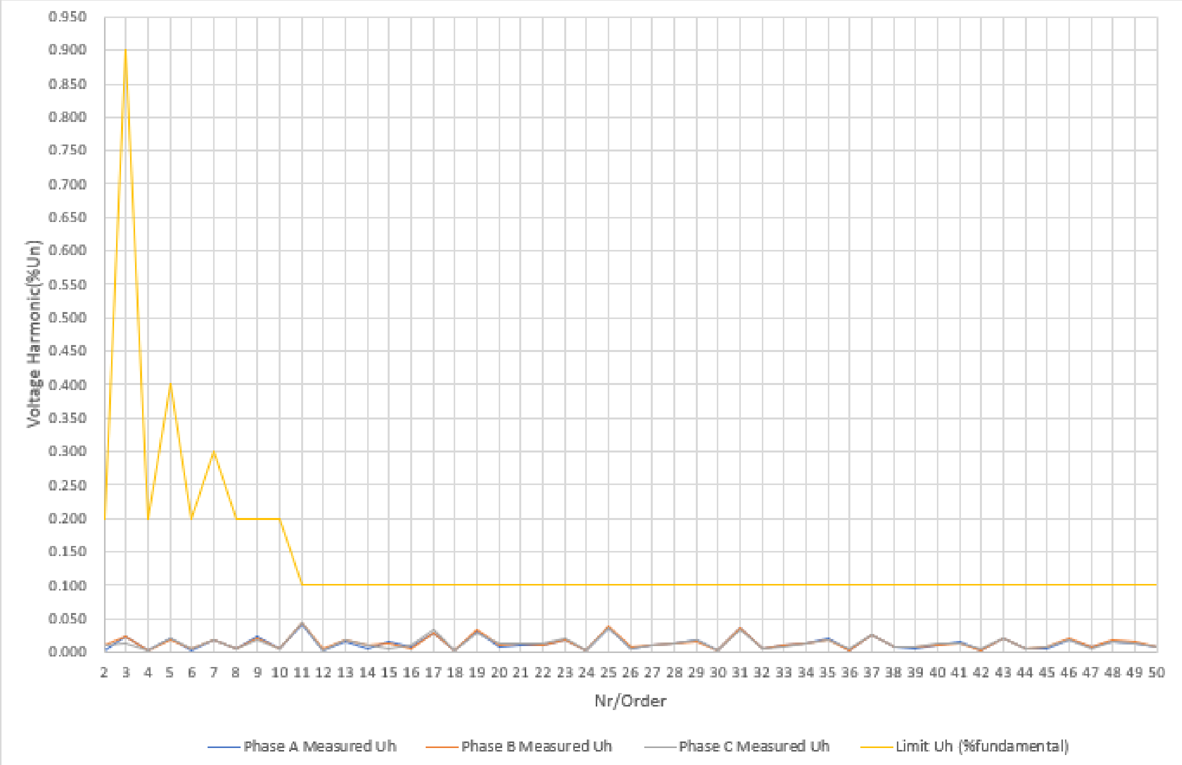
Voltage Source Harmonics at 50%Pn				
Nr/Order	**Limit U_h (%fundamental)**	**Phase A Measured U_h (%fundamental)**	**Phase B Measured Uh (%fundamental)**	**Phase C Measured Uh (%fundamental)**
2	0.200	0.003	0.009	0.011
3	0.900	0.022	0.024	0.013
4	0.200	0.003	0.003	0.004
5	0.400	0.020	0.018	0.021
6	0.200	0.003	0.004	0.006
7	0.300	0.018	0.018	0.018
8	0.200	0.006	0.006	0.006
9	0.200	0.022	0.021	0.017
10	0.200	0.006	0.005	0.005
11	0.100	0.041	0.043	0.043
12	0.100	0.003	0.005	0.004
13	0.100	0.015	0.018	0.017
14	0.100	0.006	0.010	0.009
15	0.100	0.015	0.013	0.006
16	0.100	0.008	0.006	0.009
17	0.100	0.030	0.030	0.034
18	0.100	0.003	0.003	0.003
19	0.100	0.031	0.033	0.029
20	0.100	0.007	0.010	0.012
21	0.100	0.010	0.012	0.012
22	0.100	0.010	0.010	0.012
23	0.100	0.019	0.017	0.021
24	0.100	0.003	0.002	0.003
25	0.100	0.037	0.038	0.036
26	0.100	0.004	0.007	0.006
27	0.100	0.010	0.011	0.010
28	0.100	0.013	0.012	0.014
29	0.100	0.019	0.017	0.018
30	0.100	0.003	0.002	0.004
31	0.100	0.035	0.035	0.034
32	0.100	0.005	0.005	0.005
33	0.100	0.009	0.009	0.008
34	0.100	0.013	0.013	0.014
35	0.100	0.020	0.019	0.019
36	0.100	0.003	0.003	0.004
37	0.100	0.026	0.026	0.026
38	0.100	0.008	0.007	0.007
39	0.100	0.006	0.007	0.007
40	0.100	0.011	0.011	0.012
41	0.100	0.014	0.014	0.013
42	0.100	0.003	0.003	0.004
43	0.100	0.020	0.021	0.020
44	0.100	0.006	0.006	0.006
45	0.100	0.006	0.007	0.007
46	0.100	0.019	0.020	0.019
47	0.100	0.007	0.007	0.006

Voltage Source Harmonics at 50%Pn				
Nr/Order	**Limit U_h (%fundamental)**	**Phase A Measured U_h (%fundamental)**	**Phase B Measured Uh (%fundamental)**	**Phase C Measured Uh (%fundamental)**
48	0.100	0.016	0.018	0.017
49	0.100	0.014	0.014	0.014
50	0.100	0.009	0.009	0.008
THD((%fundamental)	5.000	0.114	0.117	0.114

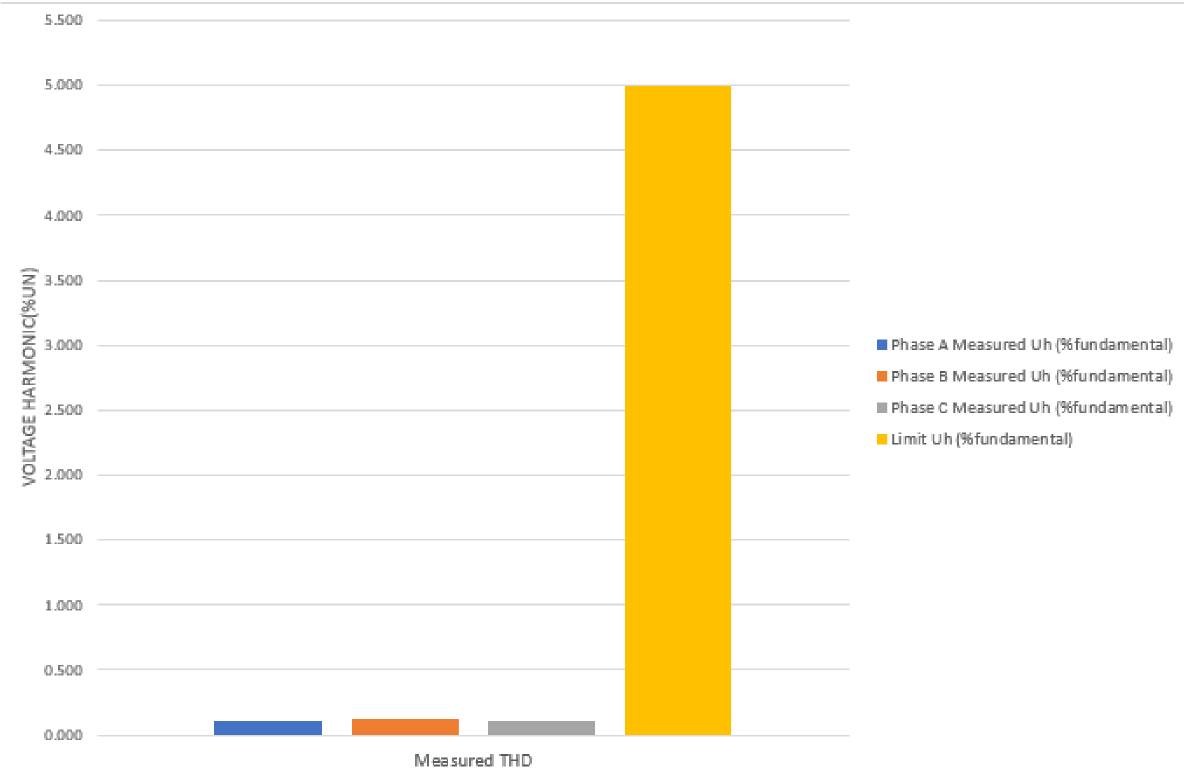
Voltage Source Harmonics at 100%Pn				
Nr/Order	**Limit U_h (%fundamental)**	**Phase A Measured U_h (%fundamental)**	**Phase B Measured Uh (%fundamental)**	**Phase C Measured Uh (%fundamental)**
2	0.200	0.004	0.009	0.011
3	0.900	0.080	0.077	0.077
4	0.200	0.003	0.007	0.014
5	0.400	0.022	0.021	0.018
6	0.200	0.003	0.005	0.007
7	0.300	0.036	0.036	0.029
8	0.200	0.004	0.007	0.007
9	0.200	0.009	0.010	0.005
10	0.200	0.003	0.004	0.003
11	0.100	0.036	0.037	0.037
12	0.100	0.003	0.003	0.004
13	0.100	0.015	0.017	0.017
14	0.100	0.003	0.004	0.004
15	0.100	0.020	0.023	0.015
16	0.100	0.003	0.002	0.003
17	0.100	0.023	0.020	0.024
18	0.100	0.003	0.003	0.003
19	0.100	0.026	0.026	0.027
20	0.100	0.005	0.006	0.008
21	0.100	0.010	0.009	0.005
22	0.100	0.004	0.004	0.004
23	0.100	0.017	0.016	0.018
24	0.100	0.002	0.003	0.002
25	0.100	0.028	0.030	0.029
26	0.100	0.003	0.004	0.004
27	0.100	0.017	0.016	0.010
28	0.100	0.006	0.005	0.006
29	0.100	0.018	0.015	0.017
30	0.100	0.002	0.002	0.002
31	0.100	0.028	0.028	0.029
32	0.100	0.002	0.003	0.003
33	0.100	0.014	0.011	0.008
34	0.100	0.007	0.006	0.007
35	0.100	0.018	0.015	0.017
36	0.100	0.003	0.003	0.003
37	0.100	0.025	0.026	0.026
38	0.100	0.004	0.004	0.005
39	0.100	0.014	0.012	0.010
40	0.100	0.007	0.007	0.008
41	0.100	0.024	0.021	0.024
42	0.100	0.003	0.003	0.003
43	0.100	0.020	0.022	0.022
44	0.100	0.006	0.005	0.006
45	0.100	0.013	0.010	0.009

Voltage Source Harmonics at 100%Pn				
Nr/Order	Limit U_h (%fundamental)	Phase A Measured U_h (%fundamental)	Phase B Measured Uh (%fundamental)	Phase C Measured Uh (%fundamental)
46	0.100	0.015	0.017	0.016
47	0.100	0.022	0.019	0.020
48	0.100	0.015	0.018	0.016
49	0.100	0.021	0.022	0.022
50	0.100	0.006	0.007	0.006
THD((%fundamental)	5.000	0.135	0.133	0.131

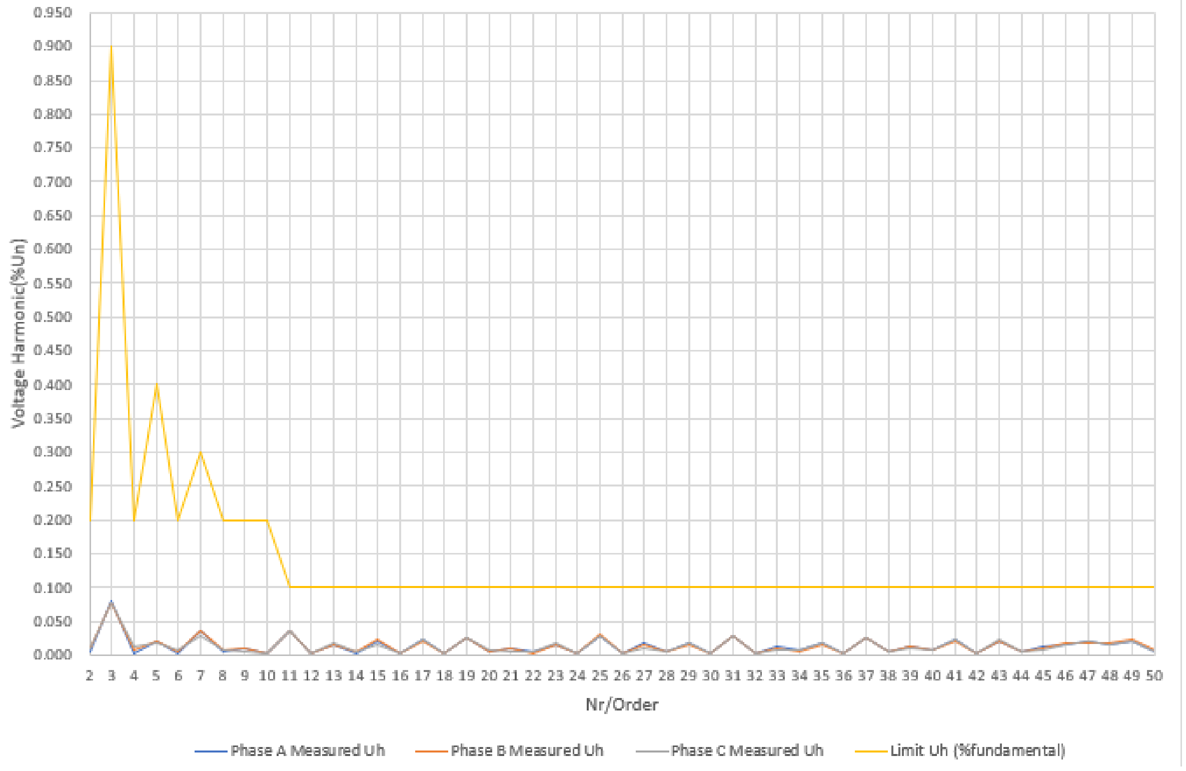
Voltage Source Harmonics at 50%Pn



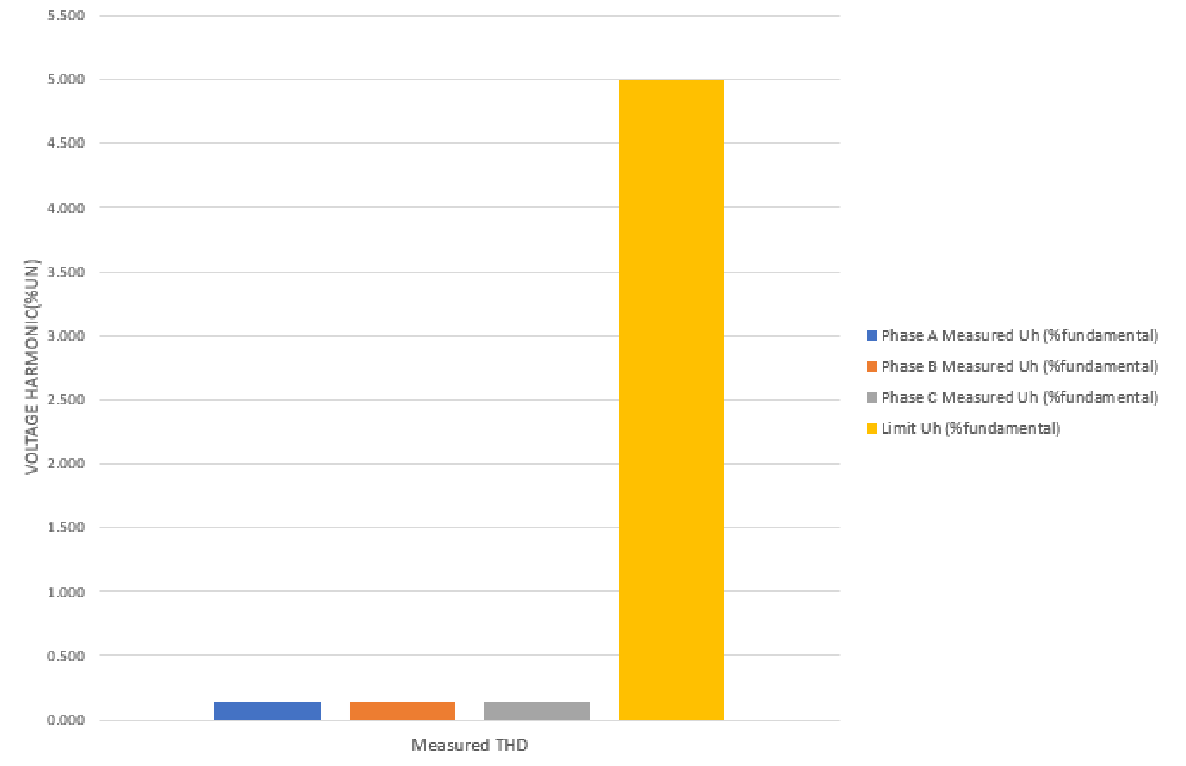
Voltage THD at 50%Pn



Voltage Source Harmonics at 100%Pn



Voltage THD at 100%Pn



4.8 FLICKERS IN CONTINUOUS OPERATION

Measurements of voltage fluctuations in continuous operation have been measured according to the Clause 5.7 of the standard.

Limits considered are: 1.0 for Pst, 0.65 for Plt, 3.3% for dc and 4% for dmax measurements, according to the standard IEC 61000-3-11: 2017.

Test Results for Phase A				
Pn(%)	Limit	33 %	66 %	100 %
PST	≤ 1.0	0.061	0.044	0.058
PLT	≤ 0.65	0.053	0.032	0.053
dc [%]	≤ 3.30	0.115	0.114	0.127
dmax [%]	4	0.188	0.213	0.180

Test Results for Phase B				
Pn(%)	Limit	33 %	66 %	100 %
PST	≤ 1.0	0.142	0.139	0.135
PLT	≤ 0.65	0.140	0.137	0.135
dc [%]	≤ 3.30	0.018	0.011	0.051
dmax [%]	4	0.158	0.119	0.152

Test Results for Phase C				
Pn(%)	Limit	33 %	66 %	100 %
PST	≤ 1.0	0.053	0.048	0.043
PLT	≤ 0.65	0.050	0.046	0.041
dc [%]	≤ 3.30	0.057	0.020	0.000
dmax [%]	4	0.109	0.108	0.000

As it can be seen in the next screenshots, this test has 12 steps. The values took of Pst, Plt, dc and dmax are the most unfavorable of the 12 steps.

Running operation 33% Pn – Phase A

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.087	Pass	0.188	Pass	0.0	Pass	0.041	Pass		
2	0.085	Pass	0.159	Pass	0.0	Pass	0.039	Pass		
3	0.110	Pass	0.159	Pass	0.0	Pass	0.048	Pass		
4	0.113	Pass	0.161	Pass	0.0	Pass	0.054	Pass		
5	0.113	Pass	0.153	Pass	0.0	Pass	0.053	Pass		
6	0.115	Pass	0.136	Pass	0.0	Pass	0.058	Pass		
7	0.106	Pass	0.162	Pass	0.0	Pass	0.061	Pass		
8	0.103	Pass	0.137	Pass	0.0	Pass	0.057	Pass		
9	0.104	Pass	0.156	Pass	0.0	Pass	0.056	Pass		
10	0.097	Pass	0.134	Pass	0.0	Pass	0.054	Pass		
11	0.103	Pass	0.162	Pass	0.0	Pass	0.054	Pass		
12	0.099	Pass	0.154	Pass	0.0	Pass	0.057	Pass		
Result		Pass		Pass		Pass		Pass	0.053	Pass

Running operation 33% Pn – Phase B

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.004	Pass	0.111	Pass	0.0	Pass	0.142	Pass		
2	0.003	Pass	0.119	Pass	0.0	Pass	0.141	Pass		
3	0.011	Pass	0.101	Pass	0.0	Pass	0.140	Pass		
4	0.012	Pass	0.111	Pass	0.0	Pass	0.140	Pass		
5	0.000	Pass	0.000	Pass	0.0	Pass	0.140	Pass		
6	0.000	Pass	0.000	Pass	0.0	Pass	0.140	Pass		
7	0.000	Pass	0.000	Pass	0.0	Pass	0.139	Pass		
8	0.018	Pass	0.158	Pass	0.0	Pass	0.140	Pass		
9	0.014	Pass	0.123	Pass	0.0	Pass	0.139	Pass		
10	0.009	Pass	0.107	Pass	0.0	Pass	0.140	Pass		
11	0.006	Pass	0.102	Pass	0.0	Pass	0.139	Pass		
12	0.009	Pass	0.117	Pass	0.0	Pass	0.140	Pass		
Result		Pass		Pass		Pass		Pass	0.140	Pass

Running operation 33% Pn – Phase C

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.000	Pass	0.000	Pass	0.0	Pass	0.053	Pass		
2	0.000	Pass	0.000	Pass	0.0	Pass	0.051	Pass		
3	0.000	Pass	0.000	Pass	0.0	Pass	0.049	Pass		
4	0.000	Pass	0.000	Pass	0.0	Pass	0.050	Pass		
5	0.017	Pass	0.108	Pass	0.0	Pass	0.050	Pass		
6	0.020	Pass	0.106	Pass	0.0	Pass	0.049	Pass		
7	0.014	Pass	0.104	Pass	0.0	Pass	0.050	Pass		
8	0.057	Pass	0.109	Pass	0.0	Pass	0.050	Pass		
9	0.049	Pass	0.108	Pass	0.0	Pass	0.049	Pass		
10	0.002	Pass	0.106	Pass	0.0	Pass	0.048	Pass		
11	0.000	Pass	0.000	Pass	0.0	Pass	0.049	Pass		
12	0.000	Pass	0.000	Pass	0.0	Pass	0.049	Pass		
Result		Pass		Pass		Pass		Pass	0.050	Pass

Running operation 66% Pn – Phase A

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.114	Pass	0.159	Pass	0.0	Pass	0.044	Pass		
2	0.068	Pass	0.109	Pass	0.0	Pass	0.037	Pass		
3	0.092	Pass	0.132	Pass	0.0	Pass	0.027	Pass		
4	0.017	Pass	0.165	Pass	0.0	Pass	0.033	Pass		
5	0.098	Pass	0.213	Pass	0.0	Pass	0.025	Pass		
6	0.071	Pass	0.133	Pass	0.0	Pass	0.025	Pass		
7	0.078	Pass	0.171	Pass	0.0	Pass	0.026	Pass		
8	0.104	Pass	0.199	Pass	0.0	Pass	0.032	Pass		
9	0.036	Pass	0.151	Pass	0.0	Pass	0.027	Pass		
10	0.095	Pass	0.152	Pass	0.0	Pass	0.028	Pass		
11	0.081	Pass	0.146	Pass	0.0	Pass	0.030	Pass		
12	0.090	Pass	0.144	Pass	0.0	Pass	0.033	Pass		
Result		Pass		Pass		Pass		Pass	0.032	Pass

Running operation 66% Pn – Phase B

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.010	Pass	0.119	Pass	0.0	Pass	0.139	Pass		
2	0.007	Pass	0.111	Pass	0.0	Pass	0.138	Pass		
3	0.006	Pass	0.114	Pass	0.0	Pass	0.137	Pass		
4	0.000	Pass	0.000	Pass	0.0	Pass	0.136	Pass		
5	0.007	Pass	0.104	Pass	0.0	Pass	0.136	Pass		
6	0.009	Pass	0.103	Pass	0.0	Pass	0.137	Pass		
7	0.000	Pass	0.000	Pass	0.0	Pass	0.136	Pass		
8	0.006	Pass	0.105	Pass	0.0	Pass	0.137	Pass		
9	0.000	Pass	0.000	Pass	0.0	Pass	0.137	Pass		
10	0.011	Pass	0.104	Pass	0.0	Pass	0.136	Pass		
11	0.010	Pass	0.119	Pass	0.0	Pass	0.137	Pass		
12	0.000	Pass	0.000	Pass	0.0	Pass	0.137	Pass		
Result		Pass		Pass		Pass		Pass	0.137	Pass

Running operation 66% Pn – Phase C

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.000	Pass	0.000	Pass	0.0	Pass	0.048	Pass		
2	0.000	Pass	0.000	Pass	0.0	Pass	0.047	Pass		
3	0.013	Pass	0.101	Pass	0.0	Pass	0.046	Pass		
4	0.009	Pass	0.101	Pass	0.0	Pass	0.045	Pass		
5	0.000	Pass	0.000	Pass	0.0	Pass	0.046	Pass		
6	0.000	Pass	0.000	Pass	0.0	Pass	0.046	Pass		
7	0.000	Pass	0.000	Pass	0.0	Pass	0.046	Pass		
8	0.000	Pass	0.000	Pass	0.0	Pass	0.046	Pass		
9	0.000	Pass	0.000	Pass	0.0	Pass	0.046	Pass		
10	0.020	Pass	0.108	Pass	0.0	Pass	0.046	Pass		
11	0.000	Pass	0.000	Pass	0.0	Pass	0.047	Pass		
12	0.000	Pass	0.000	Pass	0.0	Pass	0.047	Pass		
Result		Pass		Pass		Pass		Pass	0.046	Pass

Running operation 100% Pn – Phase A

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.103	Pass	0.139	Pass	0.0	Pass	0.058	Pass		
2	0.100	Pass	0.140	Pass	0.0	Pass	0.056	Pass		
3	0.112	Pass	0.141	Pass	0.0	Pass	0.055	Pass		
4	0.103	Pass	0.132	Pass	0.0	Pass	0.054	Pass		
5	0.091	Pass	0.144	Pass	0.0	Pass	0.054	Pass		
6	0.100	Pass	0.168	Pass	0.0	Pass	0.053	Pass		
7	0.096	Pass	0.139	Pass	0.0	Pass	0.052	Pass		
8	0.107	Pass	0.180	Pass	0.0	Pass	0.053	Pass		
9	0.107	Pass	0.173	Pass	0.0	Pass	0.052	Pass		
10	0.127	Pass	0.173	Pass	0.0	Pass	0.052	Pass		
11	0.112	Pass	0.137	Pass	0.0	Pass	0.052	Pass		
12	0.102	Pass	0.155	Pass	0.0	Pass	0.052	Pass		
Result		Pass		Pass		Pass		Pass	0.053	Pass

Running operation 100% Pn – Phase B

	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.014	Pass	0.106	Pass	0.0	Pass	0.135	Pass		
2	0.008	Pass	0.105	Pass	0.0	Pass	0.135	Pass		
3	0.010	Pass	0.110	Pass	0.0	Pass	0.134	Pass		
4	0.005	Pass	0.120	Pass	0.0	Pass	0.135	Pass		
5	0.032	Pass	0.112	Pass	0.0	Pass	0.135	Pass		
6	0.051	Pass	0.152	Pass	0.0	Pass	0.135	Pass		
7	0.000	Pass	0.000	Pass	0.0	Pass	0.134	Pass		
8	0.007	Pass	0.101	Pass	0.0	Pass	0.134	Pass		
9	0.003	Pass	0.109	Pass	0.0	Pass	0.134	Pass		
10	0.008	Pass	0.112	Pass	0.0	Pass	0.135	Pass		
11	0.000	Pass	0.000	Pass	0.0	Pass	0.134	Pass		
12	0.000	Pass	0.000	Pass	0.0	Pass	0.134	Pass		
Result		Pass		Pass		Pass		Pass	0.135	Pass

Running operation 100% Pn – Phase C

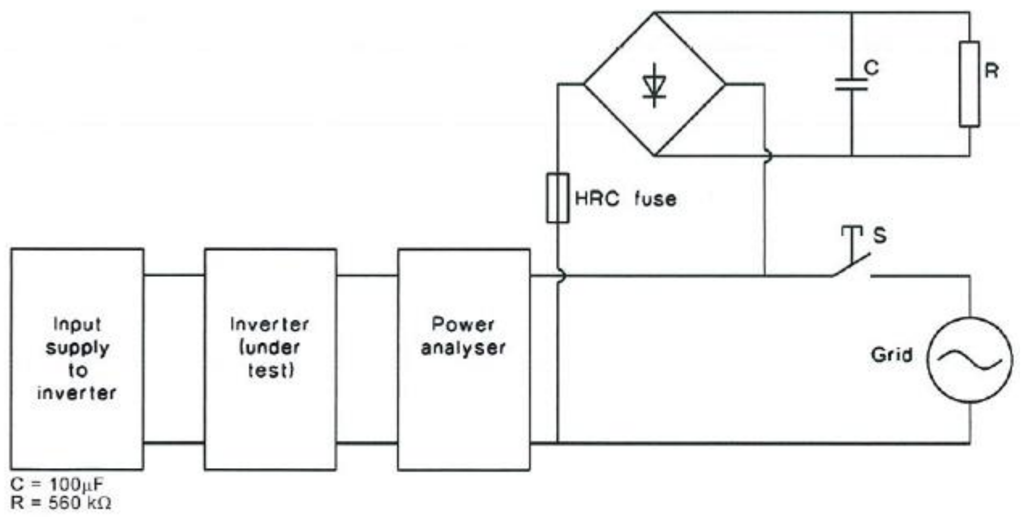
	dc[%]		dmax[%]		d(t)[ms]		Pst		Plt	
Limit	3.30		4.00		500 3.30%		1.00		0.65 N:12	
No. 1	0.000	Pass	0.000	Pass	0.0	Pass	0.043	Pass		
2	0.000	Pass	0.000	Pass	0.0	Pass	0.042	Pass		
3	0.000	Pass	0.000	Pass	0.0	Pass	0.042	Pass		
4	0.000	Pass	0.000	Pass	0.0	Pass	0.042	Pass		
5	0.000	Pass	0.000	Pass	0.0	Pass	0.041	Pass		
6	0.000	Pass	0.000	Pass	0.0	Pass	0.041	Pass		
7	0.000	Pass	0.000	Pass	0.0	Pass	0.041	Pass		
8	0.000	Pass	0.000	Pass	0.0	Pass	0.042	Pass		
9	0.000	Pass	0.000	Pass	0.0	Pass	0.041	Pass		
10	0.000	Pass	0.000	Pass	0.0	Pass	0.039	Pass		
11	0.000	Pass	0.000	Pass	0.0	Pass	0.040	Pass		
12	0.000	Pass	0.000	Pass	0.0	Pass	0.041	Pass		
Result		Pass		Pass		Pass		Pass	0.041	Pass

4.9 TRANSIENT VOLTAGE LIMITS

The purpose of this test is to verify that the inverter complies with the transient voltage limits specified below when the grid is disconnected from the inverter.

The transient voltage limits have been measured according to the Clause 5.8 of the standard and it has been used the following circuit:

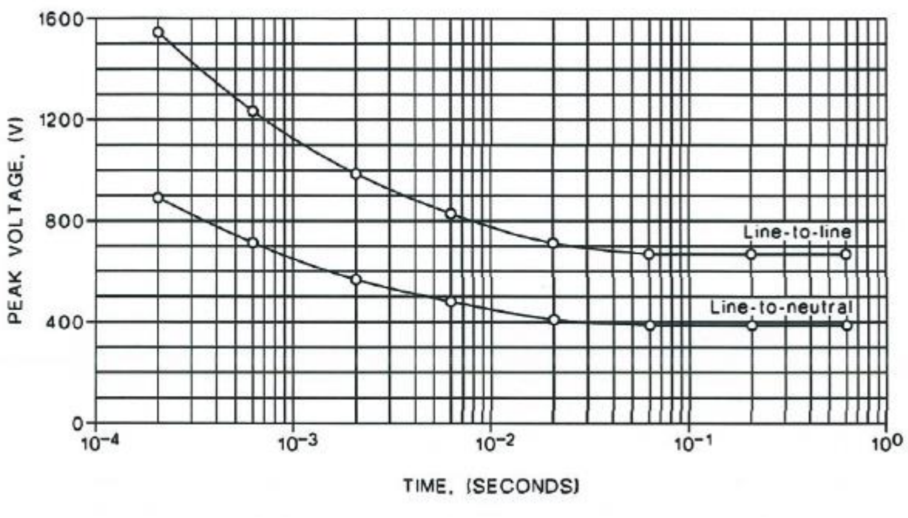
Transient Voltage Limits diagram



The resistor value per phase (R) has been calculated according to standard AS/NZS 4777.2:2015:

- The resistor is equivalent to 0.1% of the rated apparent power of the inverter.

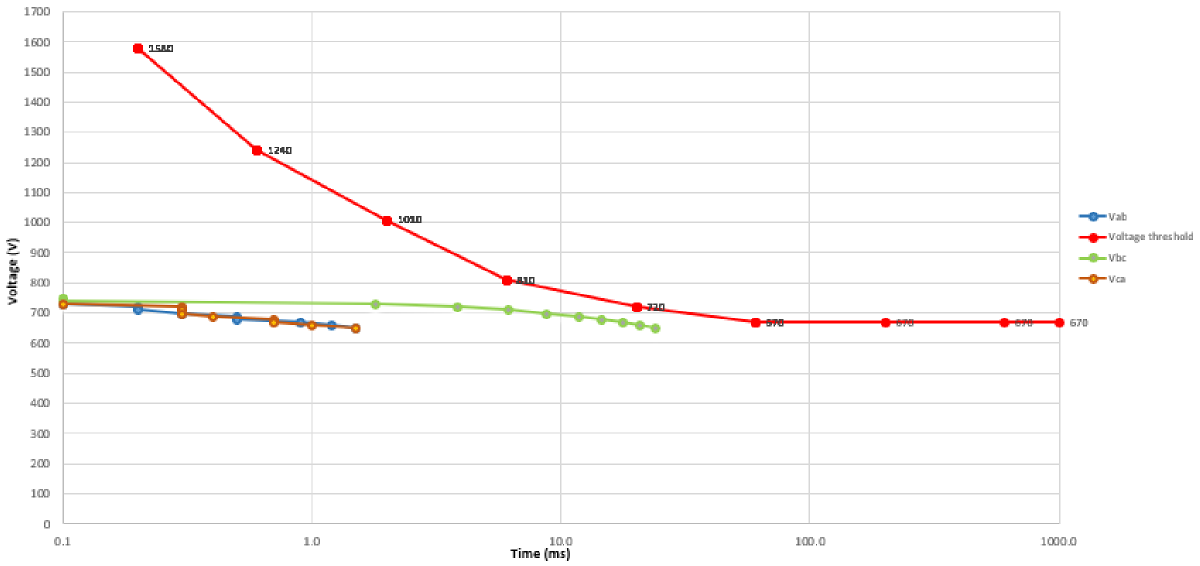
Voltage-duration Curve of transient voltage limits



Measurements have been verified at three different active power levels, 10 %Pn, 50 %Pn and 100 %Pn. Test results are offered in following pages.

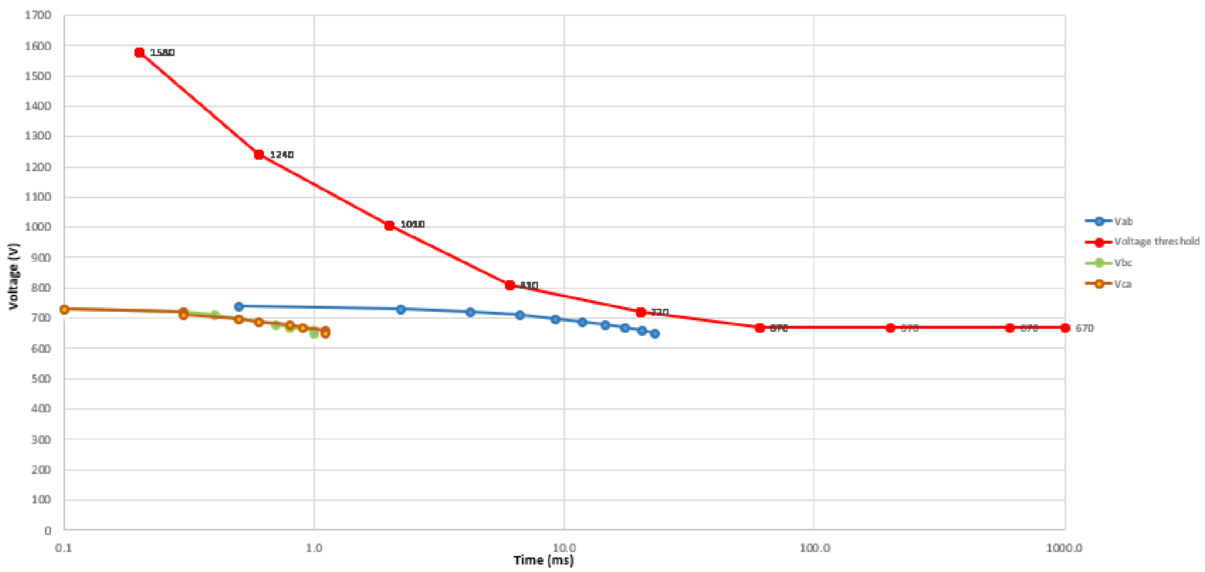
Overvoltage value measured (V) at 10% Pn					
Duration (s)	Threshold Time (ms)				RESULT
	Phase A - B	Phase B - C	Phase A - C	Limit	
0.0002	0	0	0	±1580	**P**
0.0006	0	0	0	±1240	**P**
0.002	0	0	0	±1010	**P**
0.006	0	2	0	±810	**P**
0.02	1	15	1	±720	**P**
0.06	2	24	2	±670	**P**
0.2	2	24	2	±670	**P**
0.6	2	24	2	±670	**P**

10% Pn



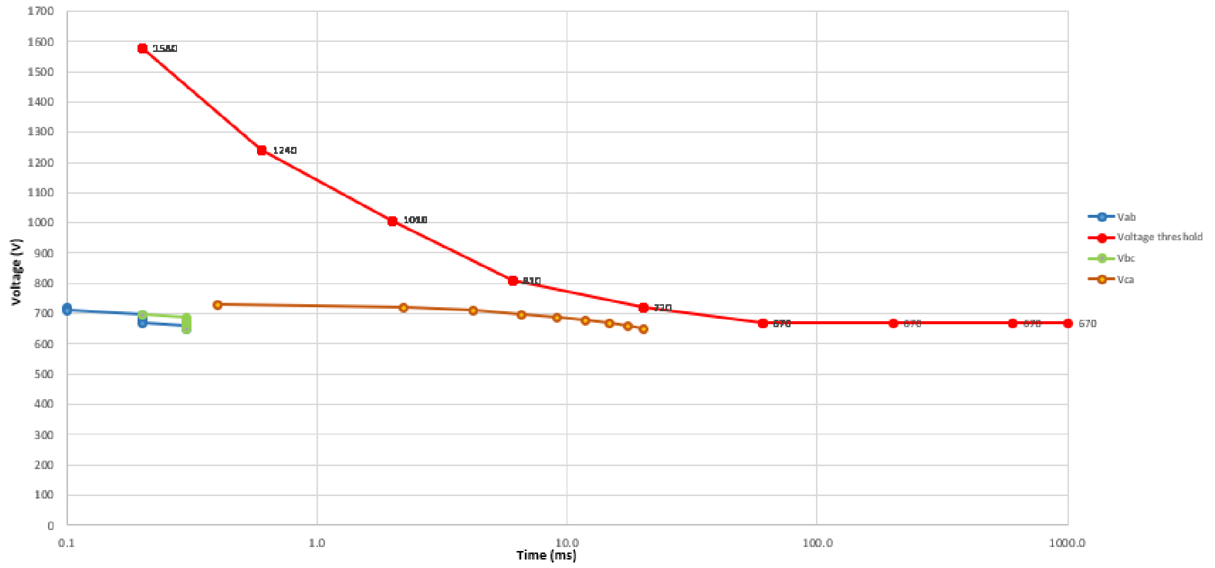
Overvoltage value measured (V) at 50% Pn					
Duration (s)	Threshold Time (ms)				RESULT
	Phase A - B	Phase B - C	Phase A - C	Limit	
0.0002	0	0	0	±1580	**P**
0.0006	0	0	0	±1240	**P**
0.002	0	0	0	±1010	**P**
0.006	2	0	0	±810	**P**
0.02	15	1	1	±720	**P**
0.06	23	1	1	±670	**P**
0.2	23	1	1	±670	**P**
0.6	23	1	1	±670	**P**

50% Pn



Overvoltage value measured (V) at 100% Pn					
Duration (s)	**Threshold Time (ms)**				**RESULT**
	Phase A - B	**Phase B - C**	**Phase A - C**	**Limit**	
0.0002	0	0	0	±1580	**P**
0.0006	0	0	0	±1240	**P**
0.002	0	0	0	±1010	**P**
0.006	0	0	0	±810	**P**
0.02	0	0	12	±720	**P**
0.06	0	0	20	±670	**P**
0.2	0	0	20	±670	**P**
0.6	0	0	20	±670	**P**

100% Pn

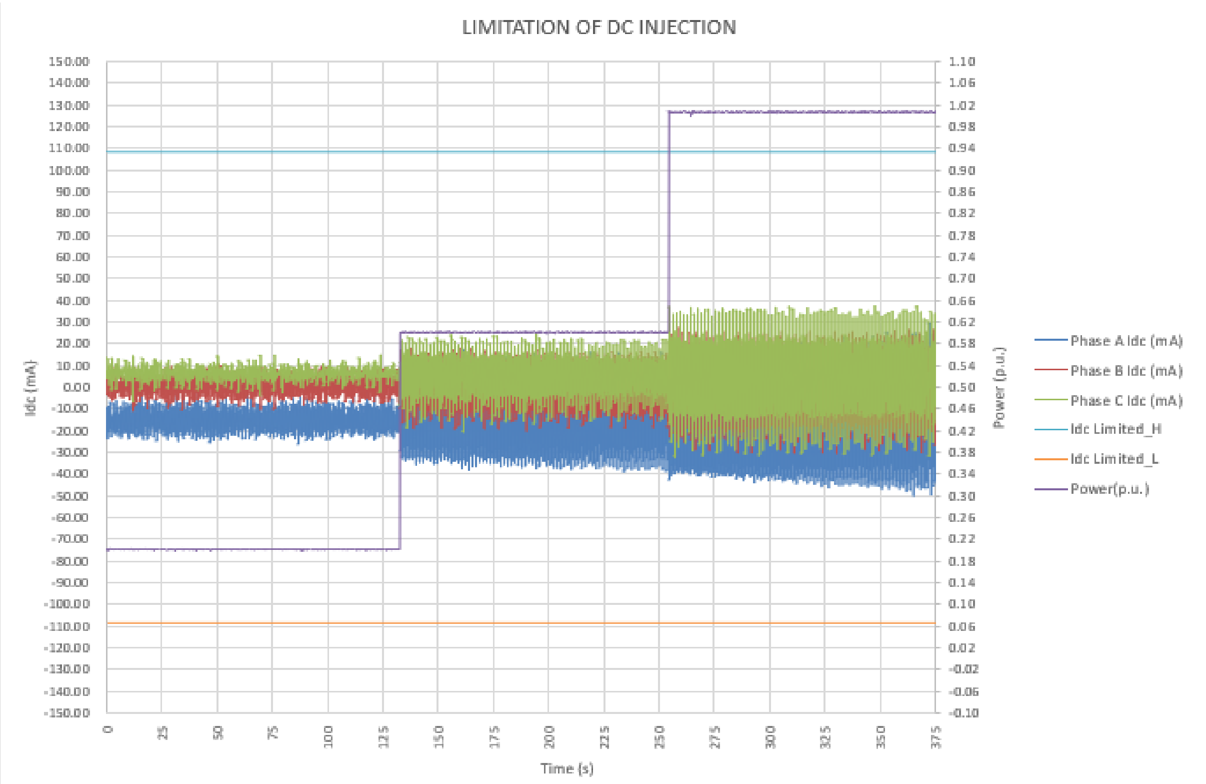


4.10 D.C. CURRENT INJECTION

The verification of DC component emission is required according to the clause 5.9 of the standard, at the specified active power levels.

	Min ~ 20%Pn	Medium ~ 60%Pn	Max ~ 100%Pn
Inverter Current Setting（A）	13.0	39.1	65.1
Inverter Current Measured（A）	13.2	39.2	65.5
Phase A Max. Test value (mA)	-26	-38	-51
Phase B Max. Test value (mA)	-11	-20	-30
Phase C Max. Test value (mA)	15	25	37
Limited (mA)	108.5	108.5	108.5
Compliance	Pass	Pass	Pass

DC Current Injection



4.11 CURRENT BALANCE FOR THREE – PHASE INVERTERS

The verification of Current Balance test has been measured according to the clause 5.10 of the standard.

It has been determined the unbalance between positive and negative sequences for voltages and currents (U_i) using following equation:

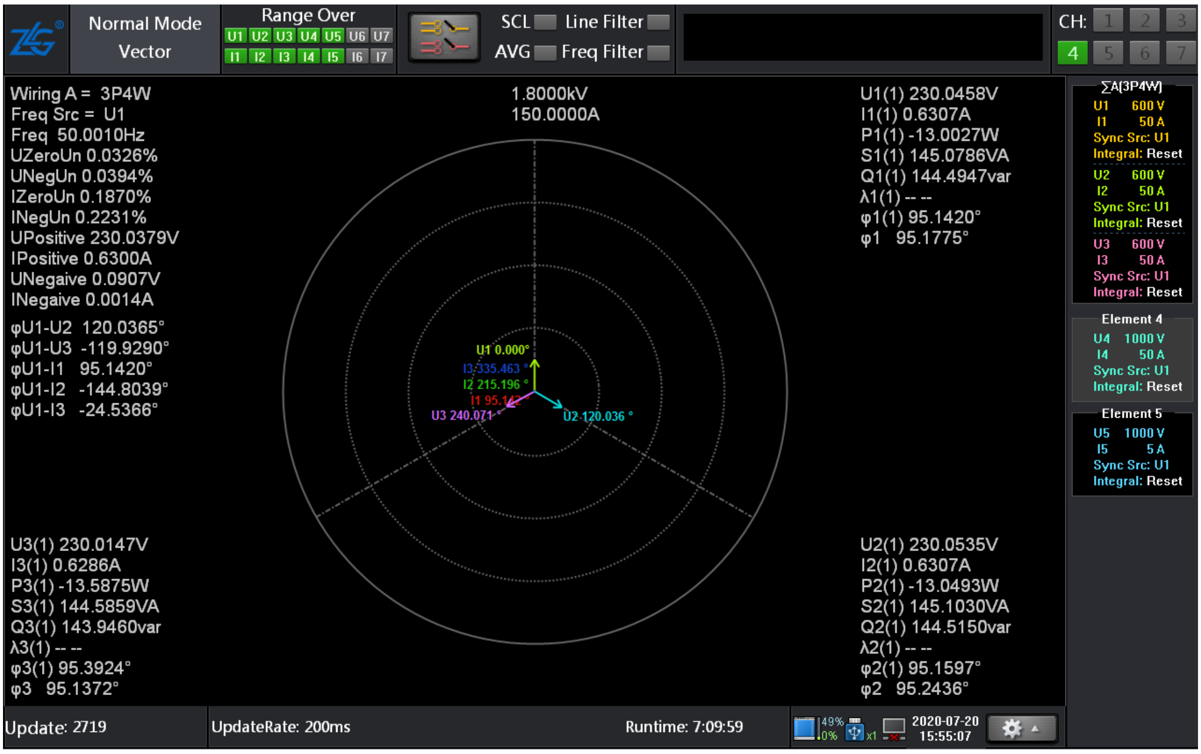
$$U_i \text{ for voltage} = (U_{1-} / U_{1+}) \cdot 100\ \%$$

$$U_i \text{ for current} = (I_{1-} / I_{1+}) \cdot 100\ \%$$

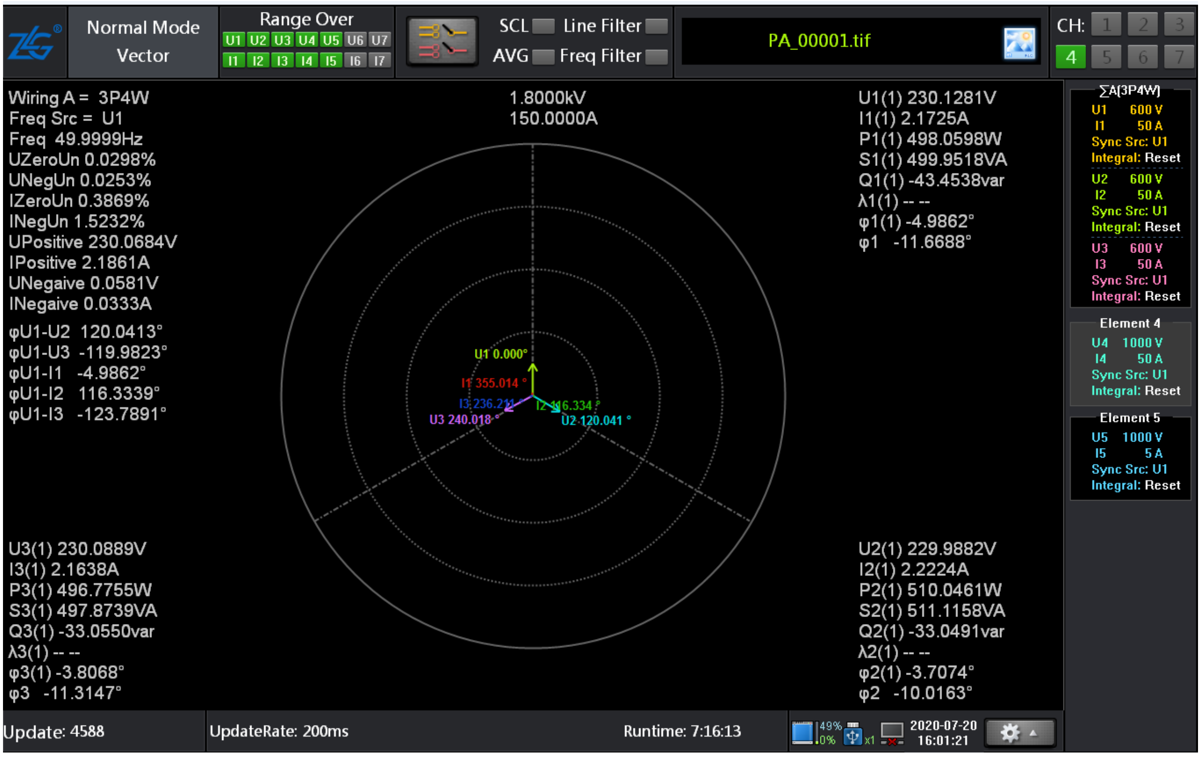
Test results represented in the table below are calculated and they represent the maximum unbalance.

P_n (%Sn)	V_{1+} (V)	V_{1-} (V)	I_{1+} (A)	I_{1-} (A)	Ui for voltage (%)	U_i for current (%)
0	230.038	0.091	0.630	0.001	0.04	0.22
10	230.068	0.058	2.186	0.033	0.03	1.52
20	230.148	0.092	4.368	0.021	0.04	0.49
30	230.187	0.090	6.558	0.029	0.04	0.44
40	230.248	0.121	8.741	0.033	0.05	0.37
50	230.397	0.049	10.937	0.018	0.02	0.16
60	230.411	0.097	13.056	0.026	0.04	0.20
70	230.432	0.056	15.160	0.021	0.02	0.14
80	230.522	0.098	17.512	0.036	0.04	0.21
90	230.655	0.132	19.582	0.053	0.06	0.27
100	230.592	0.227	21.870	0.061	0.10	0.28

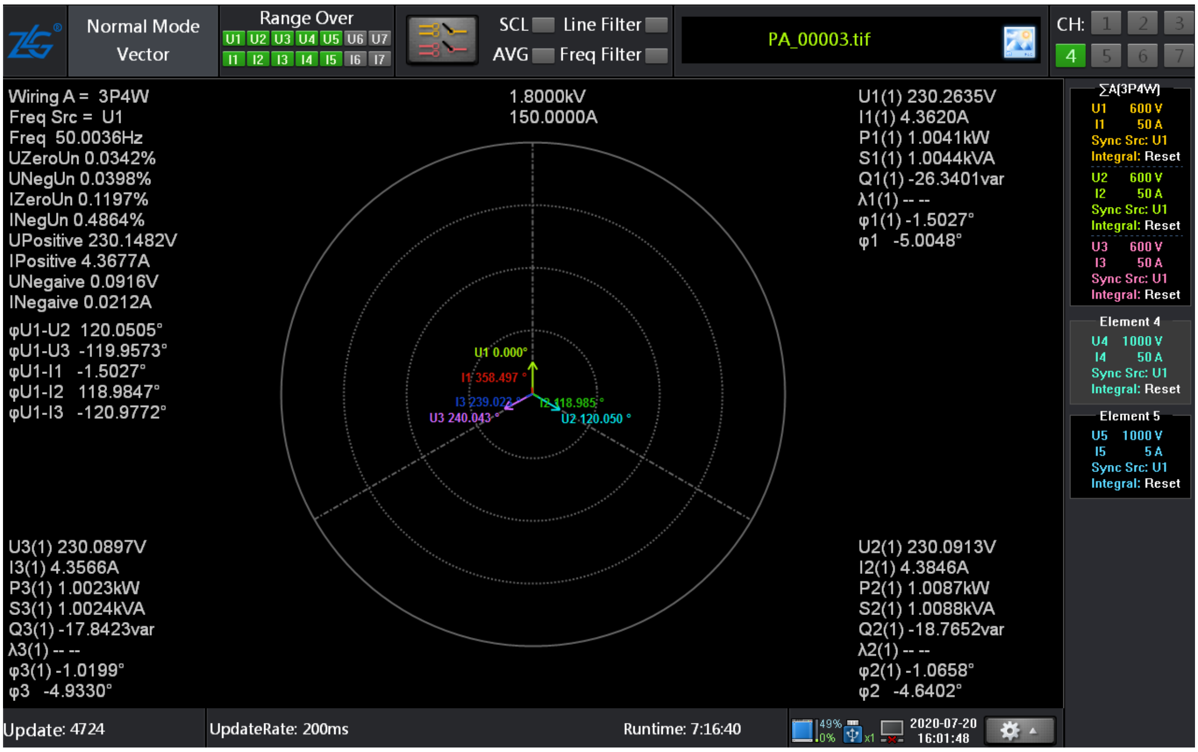
Running operation 0% Pn



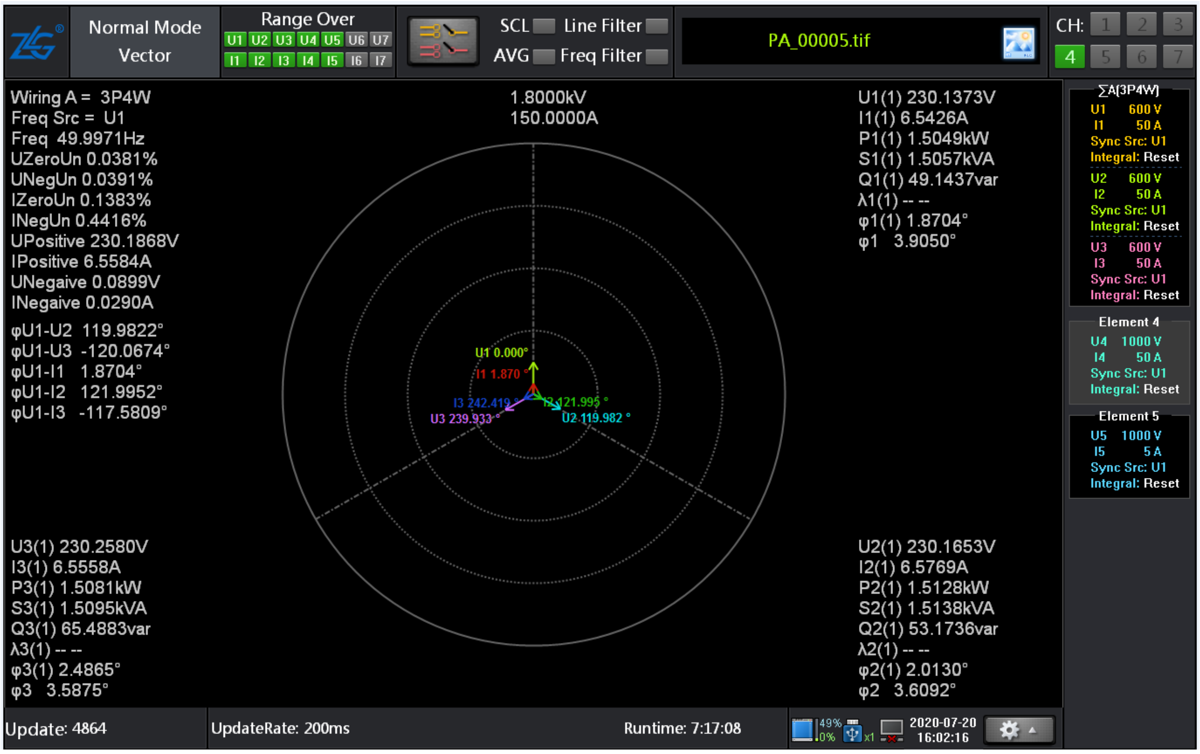
Running operation 10% Pn



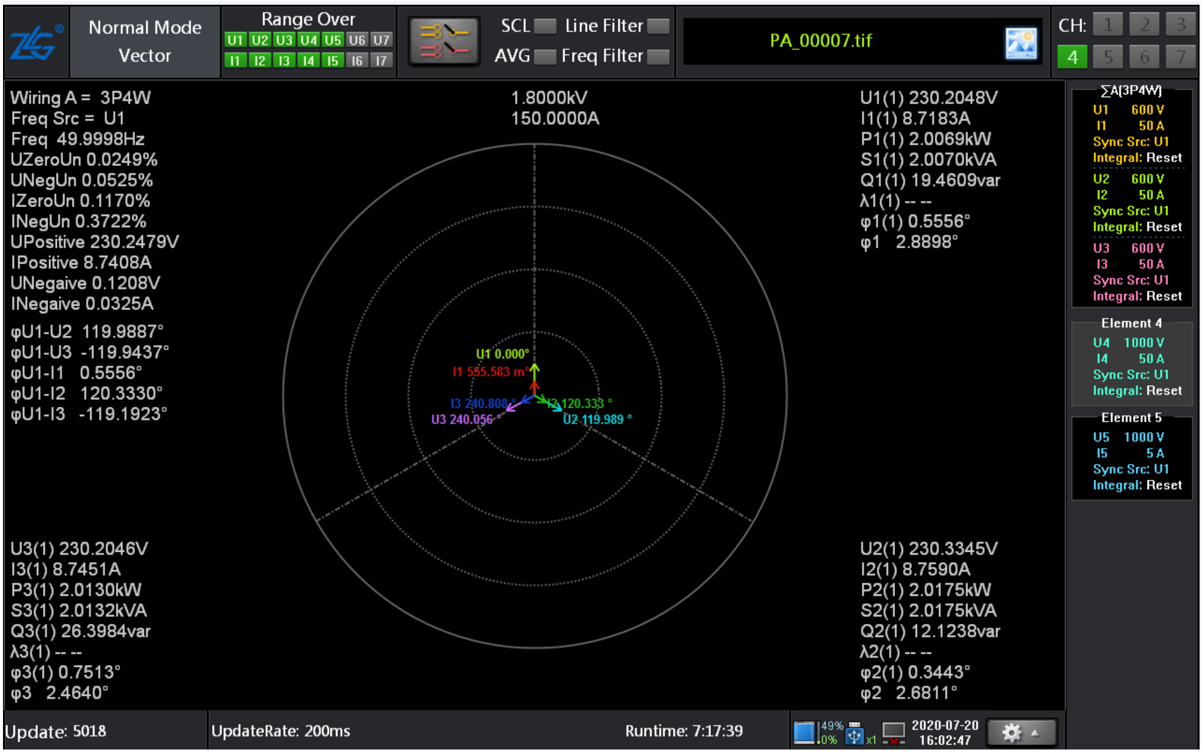
Running operation 20% Pn



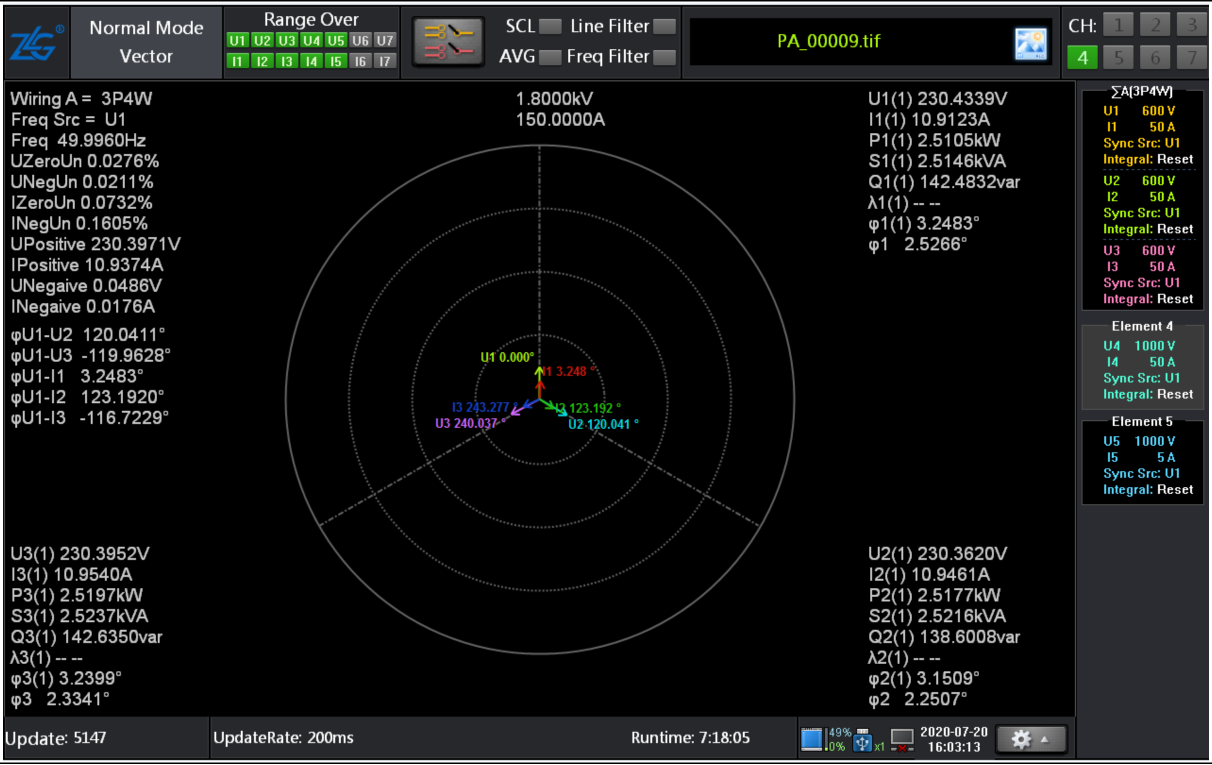
Running operation 30% Pn



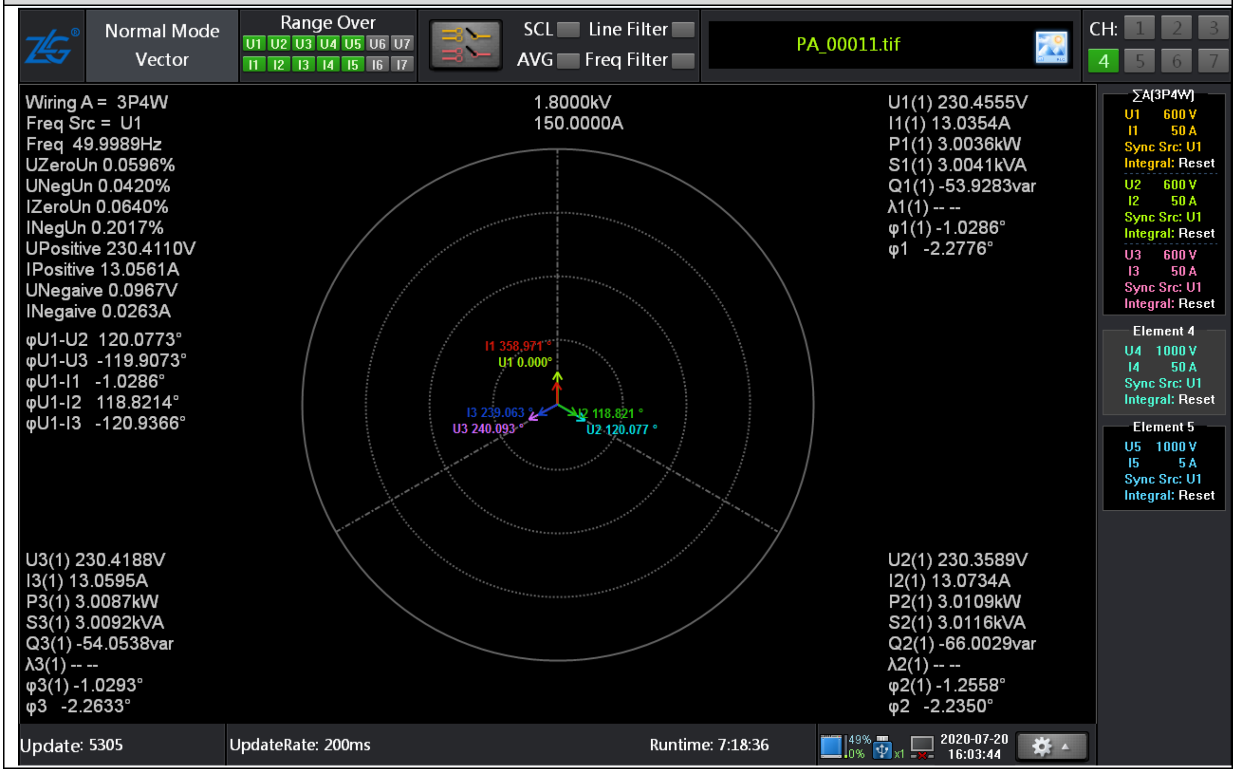
Running operation 40% Pn



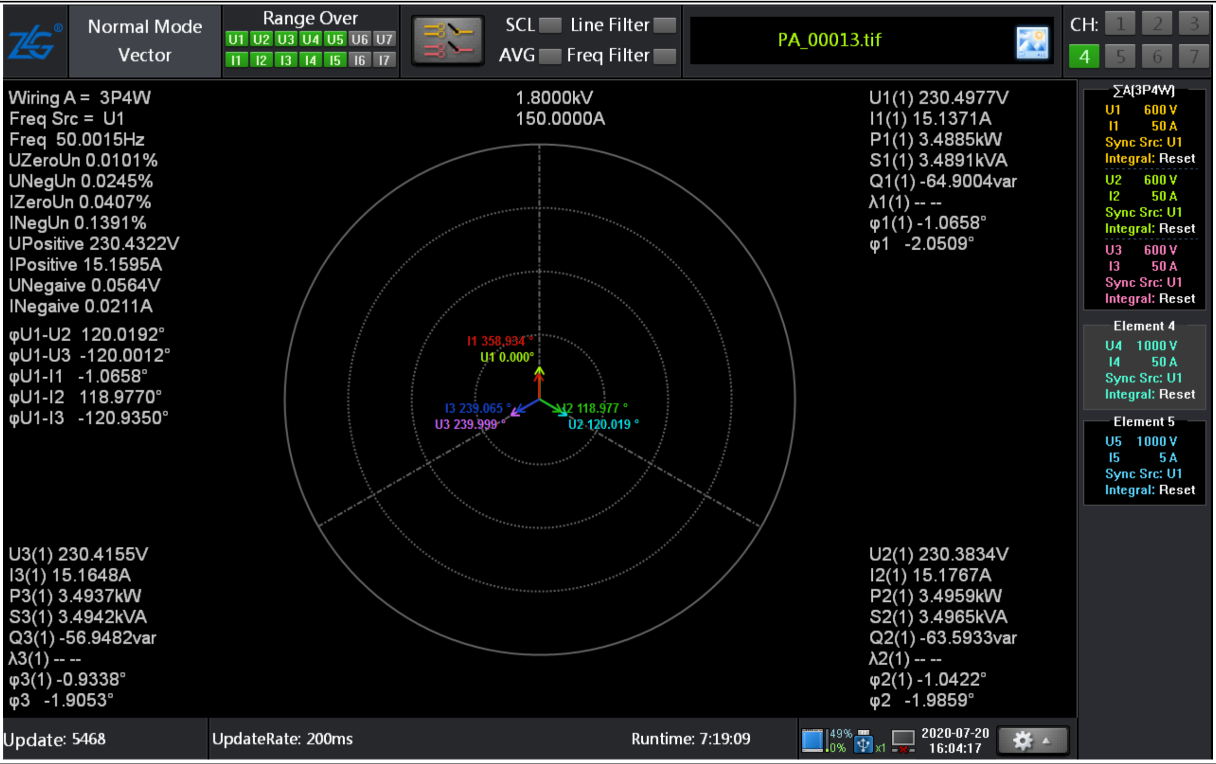
Running operation 50% Pn



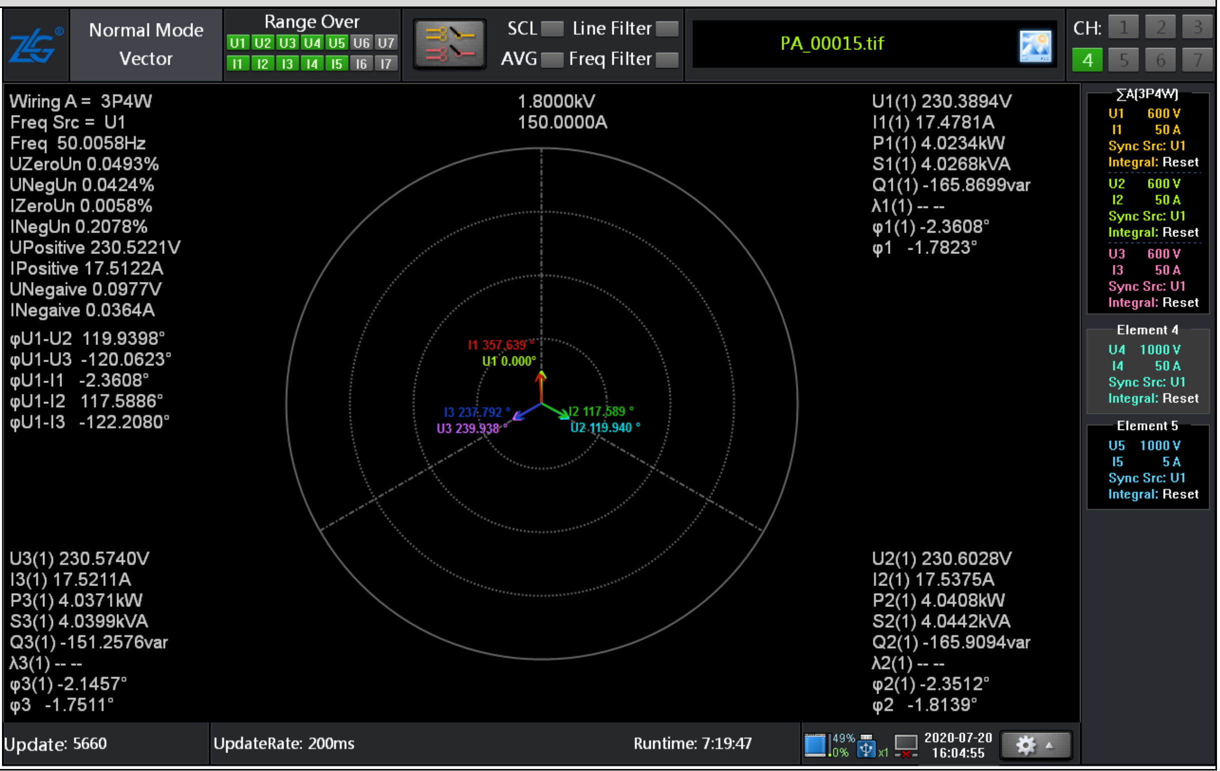
Running operation 60% Pn



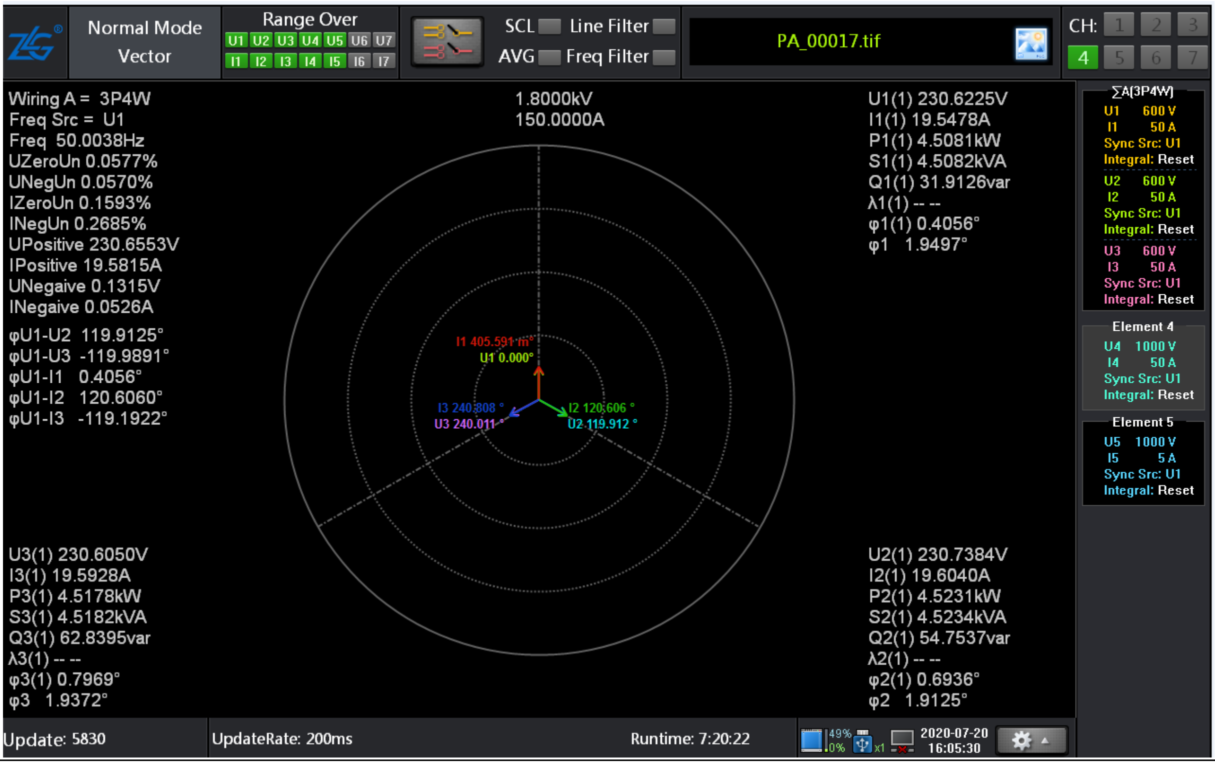
Running operation 70% Pn



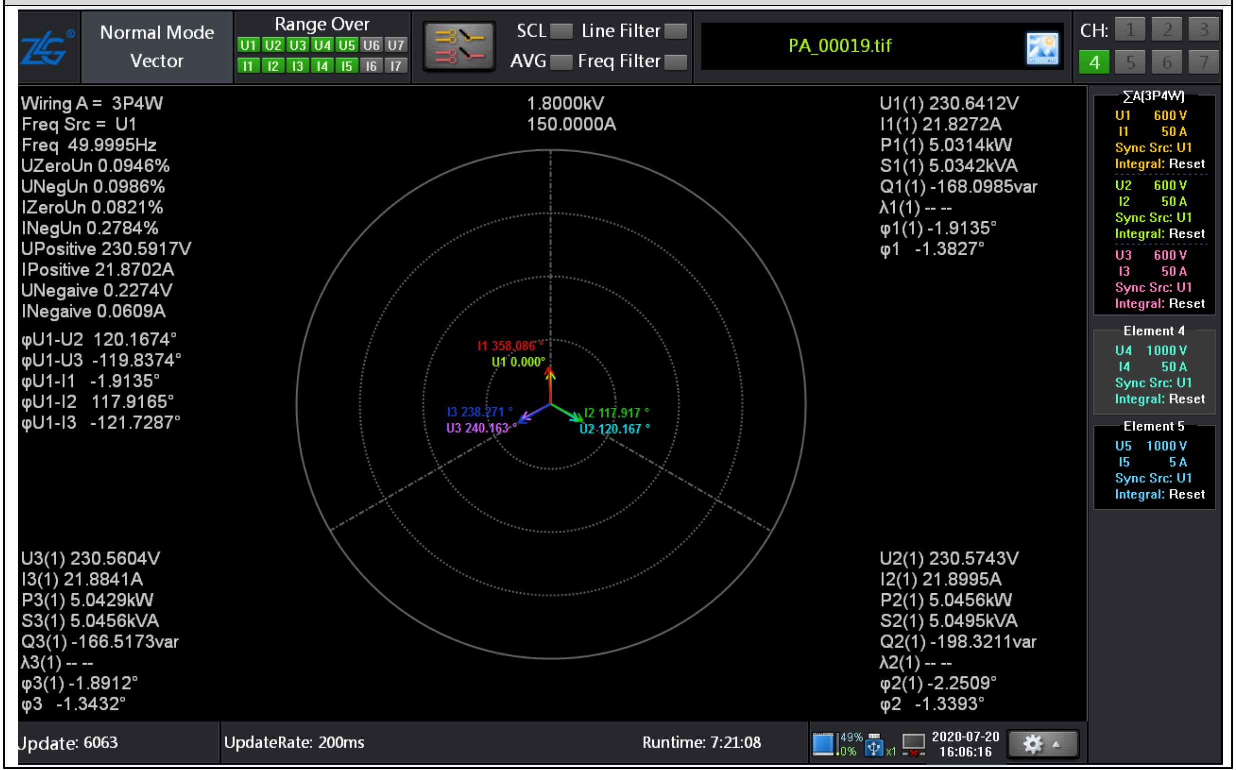
Running operation 80% Pn



Running operation 90% Pn



Running operation 100% Pn

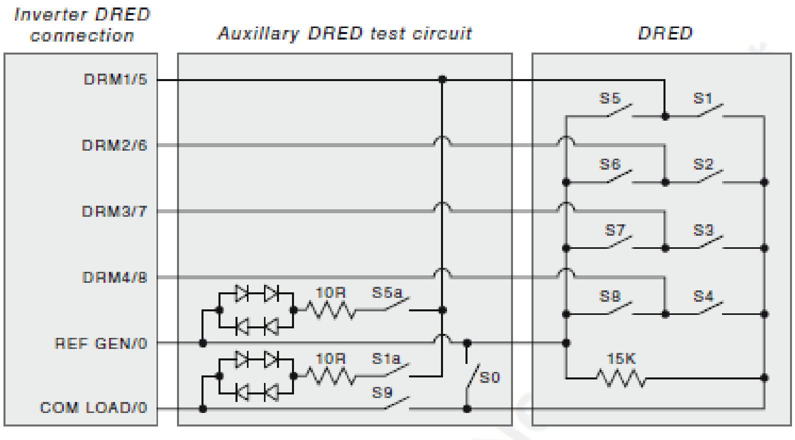


4.12 Operational Modes and Multiple Mode Inverters

4.12.1 Inverter Demand Response Modes (DRMs)

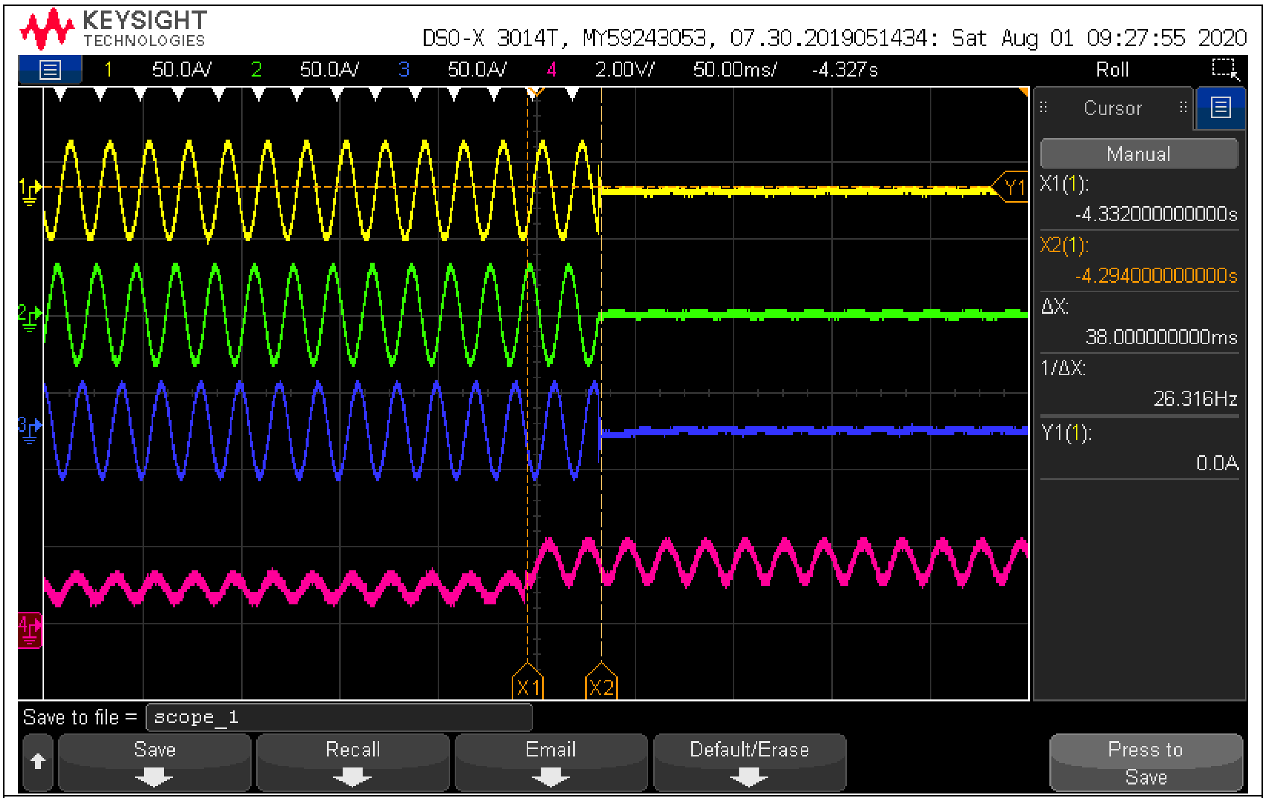
The inverter demand response mode DRM 0 has been tested according to Clause 6.2.1 of the standard. The inverter shall detect and initiate a response to the demand response commands within 2 s.

The DRED (Demand Response Enabling Device) connection circuit used for this test is:



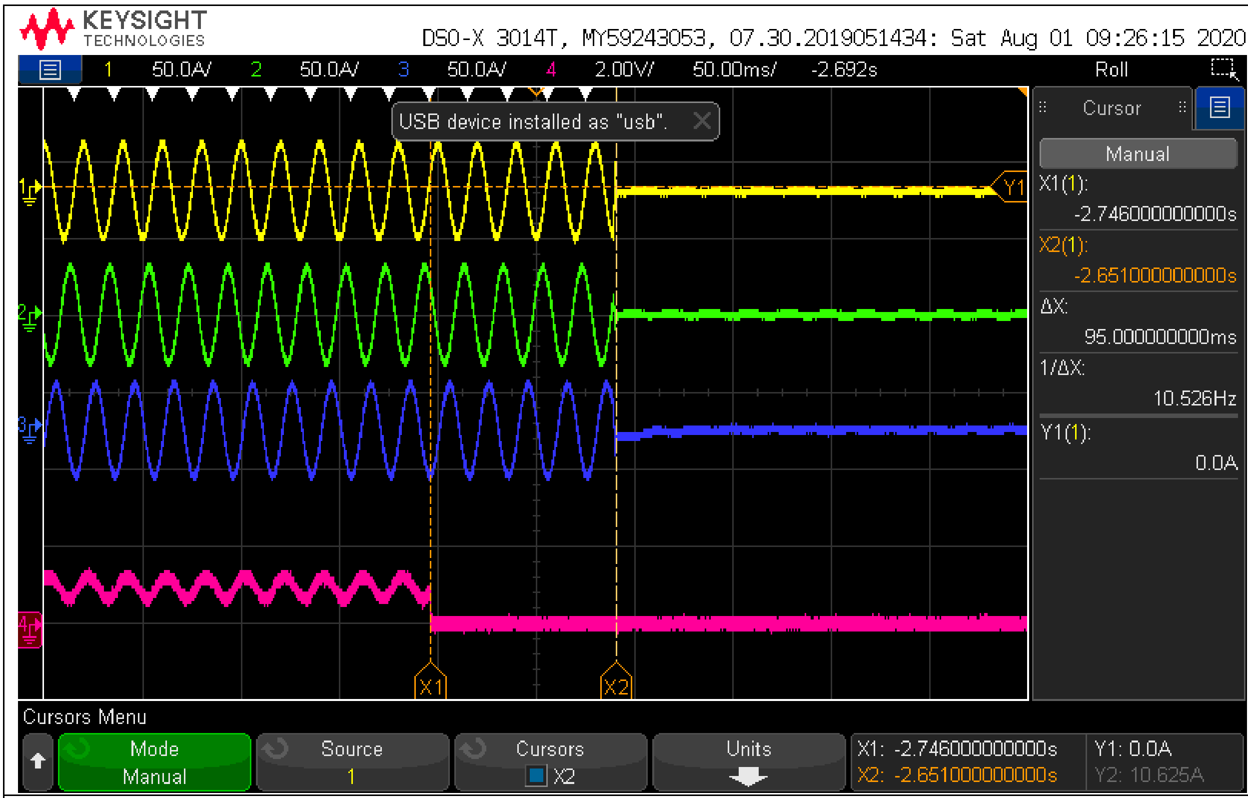
The test procedure followed has been the same as specified in the point I.2 of the standard and it is described in the following points together with test results:

a) With S9 switched closed and the inverter operating at 100% ± 5% of its rated current output, if the DRED switch S0 is asserted the unit shall disconnect.



The inverter disconnects in 38 ms

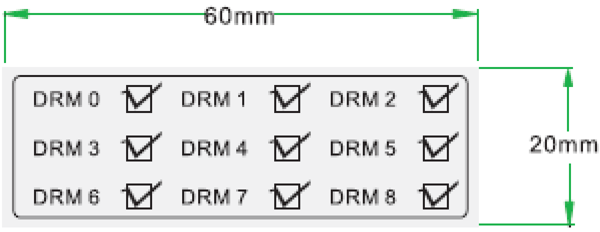
b) After reconnection disconnecting again signal S0, the switch S9 was open again and the inverter disconnected.



The inverter disconnects in 95 ms

4.12.2 Test for standard operation of generator demand response modes

The marking is showing as below:



The procedure for discharging shall be as follows:

(a) All DRM signals shall be removed and the input supply or inverter set-point shall be varied until the a.c. output of the inverter equals 100% ± 5% of its rated current output.

(b) DRED switch S7 shall be asserted and DRM 7 response assessed over a period of 2 s in accordance.

(c) DRED switch S6 shall be asserted and simultaneous DRM 6 and DRM 7 response assessed over a period of 2 s in accordance.

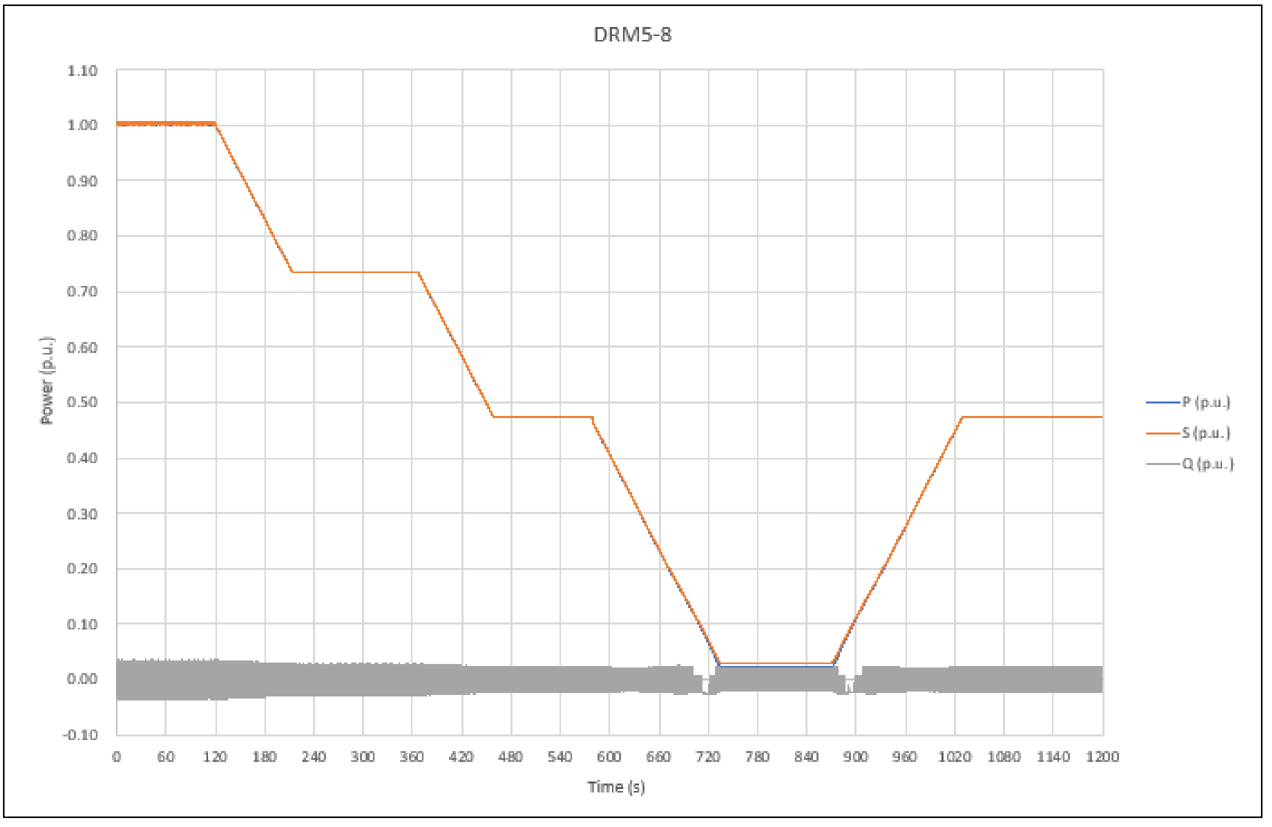
(d) DRED switch S7 shall be opened and DRM 6 response assessed over a period of 2 s in accordance

(e) DRED switch S5 shall be asserted and DRM 5 response assessed in accordance.

(f) All DRM signals shall be removed and the input supply or inverter set-point shall be varied until the a.c. output of the inverter equals 50±5% of the inverter's rated current output and is in a state able to respond to DRM 8.

(g) DRED switch S8 shall be opened and DRM 6 response assessed over a period of 2 s in accordance.

The following is the test result:



Note: Whether the slope drops or rises, the default value is 16.7%

The procedure for charging shall be as follows:

(a) All DRM signals shall be removed and the input supply or inverter set-point shall be varied until the a.c. output of the inverter equals 100% ± 5% of its rated current output.

(b) DRED switch S3 shall be asserted and DRM 3 response assessed over a period of 2 s in accordance.

(c) DRED switch S2 shall be asserted and simultaneous DRM 2 and DRM 3 response assessed over a period of 2 s in accordance.

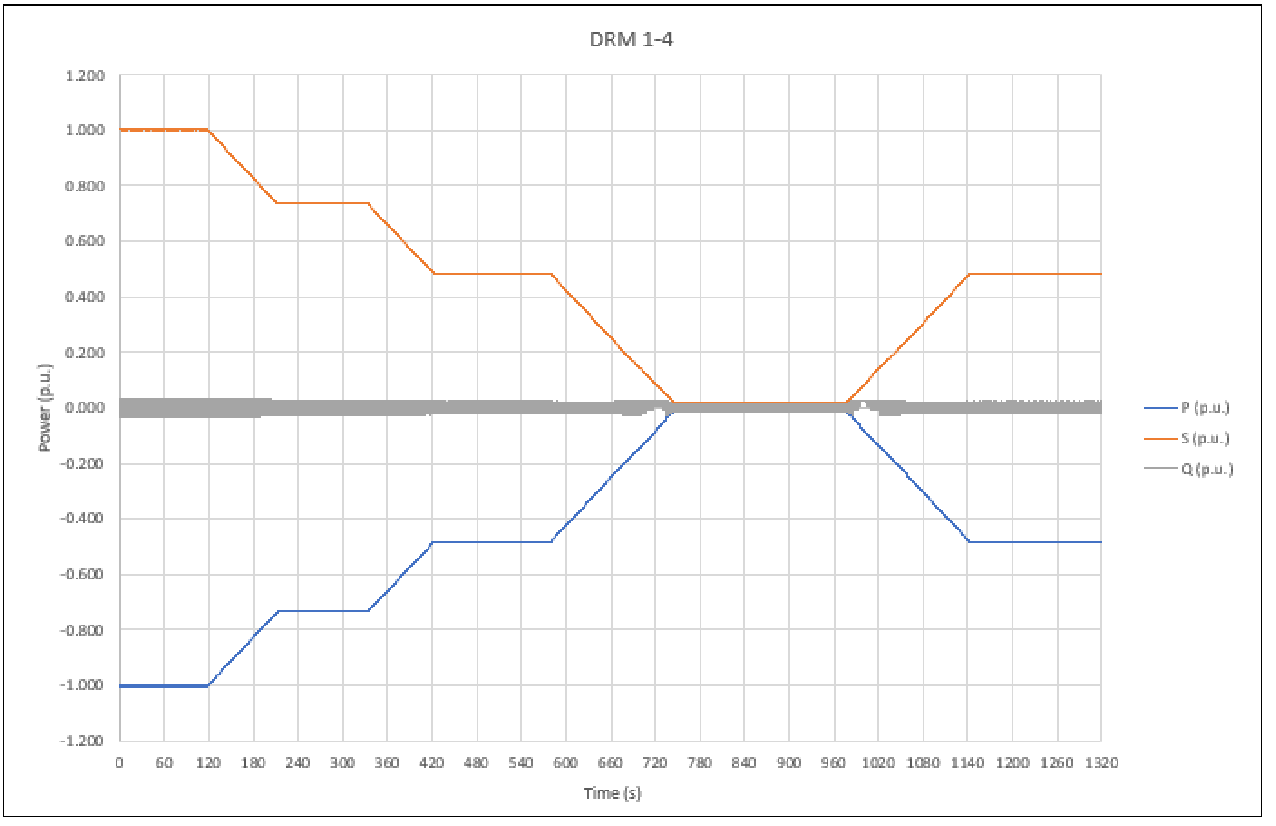
(d) DRED switch S3 shall be opened and DRM 2 response assessed over a period of 2 s in accordance

(e) DRED switch S1 shall be asserted and DRM 1 response assessed in accordance.

(f) All DRM signals shall be removed and the input supply or inverter set-point shall be varied until the a.c. output of the inverter equals 50±5% of the inverter's rated current output and is in a state able to respond to DRM 4.

(g) DRED switch S4 shall be opened and DRM 4 response assessed over a period of 2 s in accordance.

The following is the test result:



Note: Whether the slope drops or rises, the default value is 16.7%

4.12.3 Interaction with demand response enabling device (DRED)

The inverter shall have a means of connecting to a DRED. This means of connection shall include a terminal block or RJ45 socket. The terminal block or RJ45 socket shall comply with the minimum electrical specifications in Table 6. The terminal block or RJ45 socket may be physically mounted in the inverter or in a separate device that remotely communicates with the inverter.

RJ45 provided. No tests needed.

4.13 Inverter Power Quality Response Modes

The inverter power quality response modes tests have been measured according to Clause 6.3 of the standard.

The different operating modes available in the inverter and evaluated are the following:

-Volt response modes.

-Fixed power factor or reactive power mode.

-Power response mode.

-Power rate limit.

4.13.1 Volt Response Modes

Volt response modes tests have been measured according to Clause 6.3.2 of the standard.
The voltage values applied for the tests of the Clauses 6.3.2.2, 6.3.2.3 and 6.3.2.4 are the following:

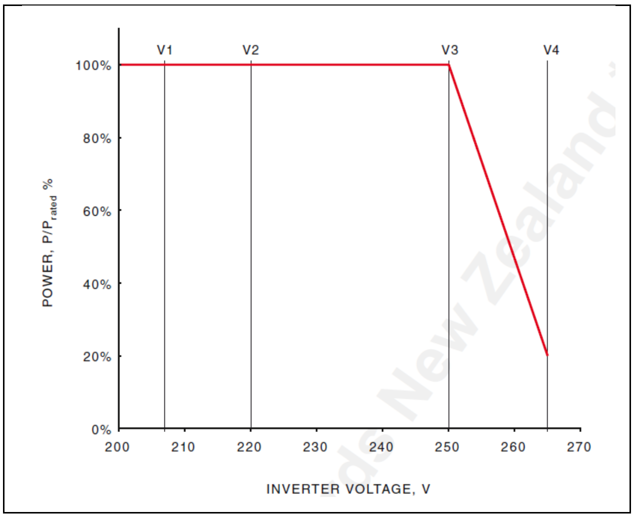
Reference	Australia. default value (V)	New Zealand. default value (V)	Range (V)
V1	207	207	Not applicable
V2	220	220	216 to 230
V3	250	244	235 to 255
V4	265	255	244 to 265

4.13.1.1 Volt – Watt Response Mode

Volt – Watt Response Mode has been measured according to Clauses 6.3.2.2 (PV Systems) at the required voltage and power points of operation.

The volt-watt response mode varies the output power of the inverter in response to the abnormal voltage at its terminal.

The curve required for volt-watt response mode for PV systems is defined by the picture below according to point 6.3.2.2 of the standard.



Two different tests have been performed to verify that the inverter volt-watt response is in accordance with the standard. These two curves tested prove also that volt-watt control function is configurable to different curves:

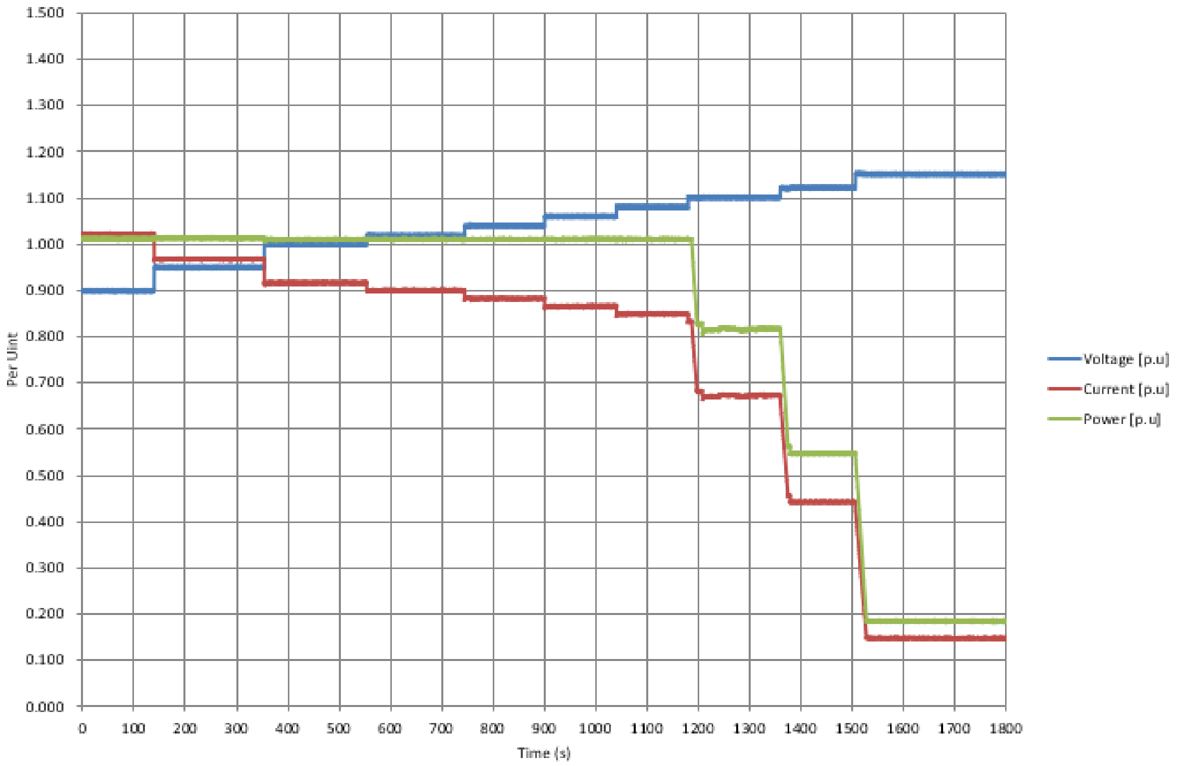
The setting values for voltage and power in the inverter have been the following:

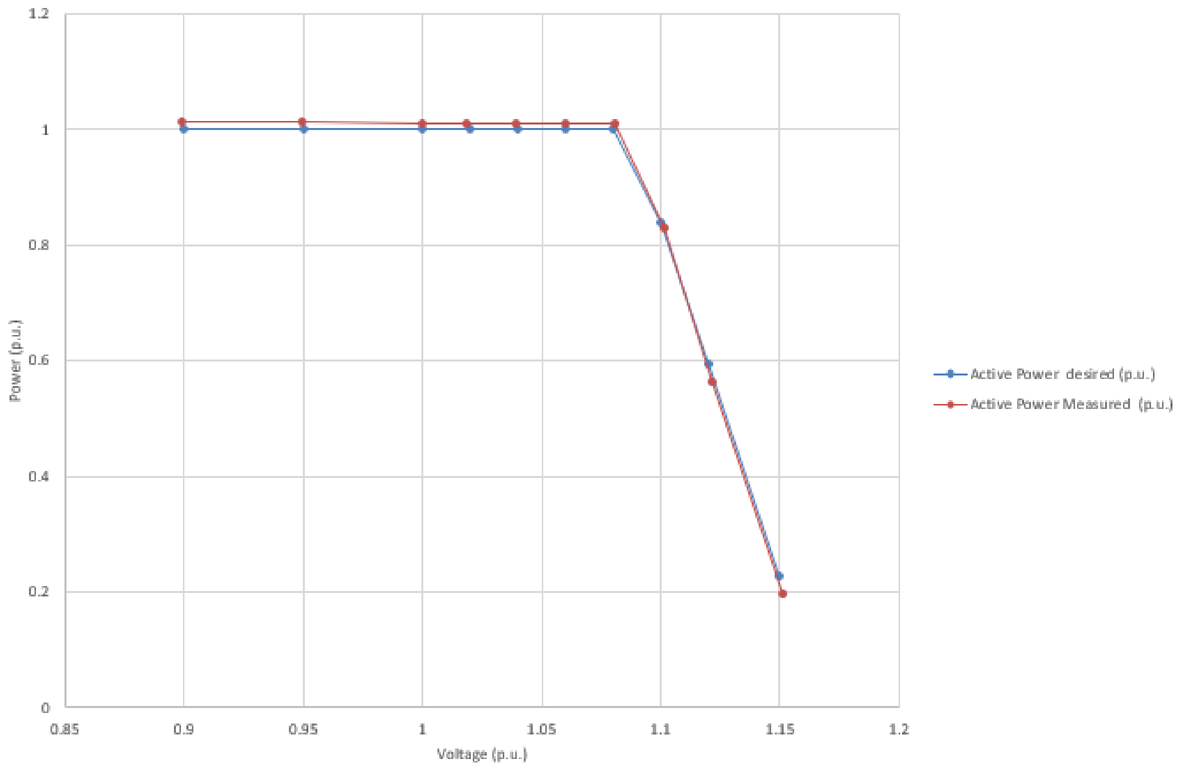
Reference	Test 1 (for Australia setting)		Test 2 (for New Zealand setting)	
	Volt. (V)	Power (%Pn)	Volt. (V)	Power (%Pn)
V1	207	100	207	100
V2	220	100	220	100
V3	250	100	244	100
V4	265	20	255	20

4.13.1.1.1 Test 1 (for Australia setting)

Voltage desired (%Un)	Voltage Measured (%Un)	Active Power desired (%Pn)	Active Power Measured (%Pn)	Active Power Deviation (%Pn)
90.0	89.9	100.0	101.2	1.2
95.0	95.0	100.0	101.3	1.3
100.0	100.0	100.0	101.0	1.0
102.0	101.9	100.0	101.0	1.0
104.0	103.9	100.0	101.1	1.1
106.0	106.0	100.0	101.1	1.1
108.0	108.0	100.0	101.1	1.1
110.0	110.1	84.0	83.0	-1.0
112.0	112.2	59.5	56.2	-3.3
115.0	115.1	22.7	19.8	-2.9

Volt – Watt (Test 1)

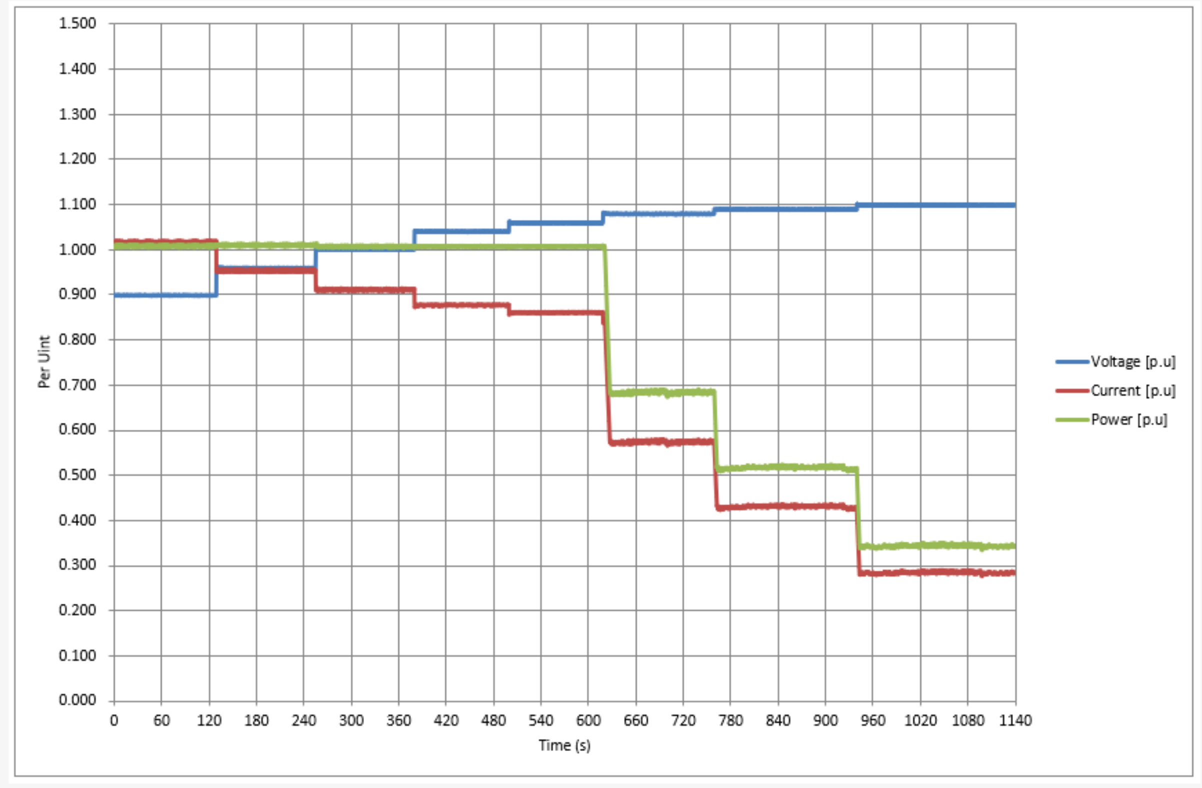


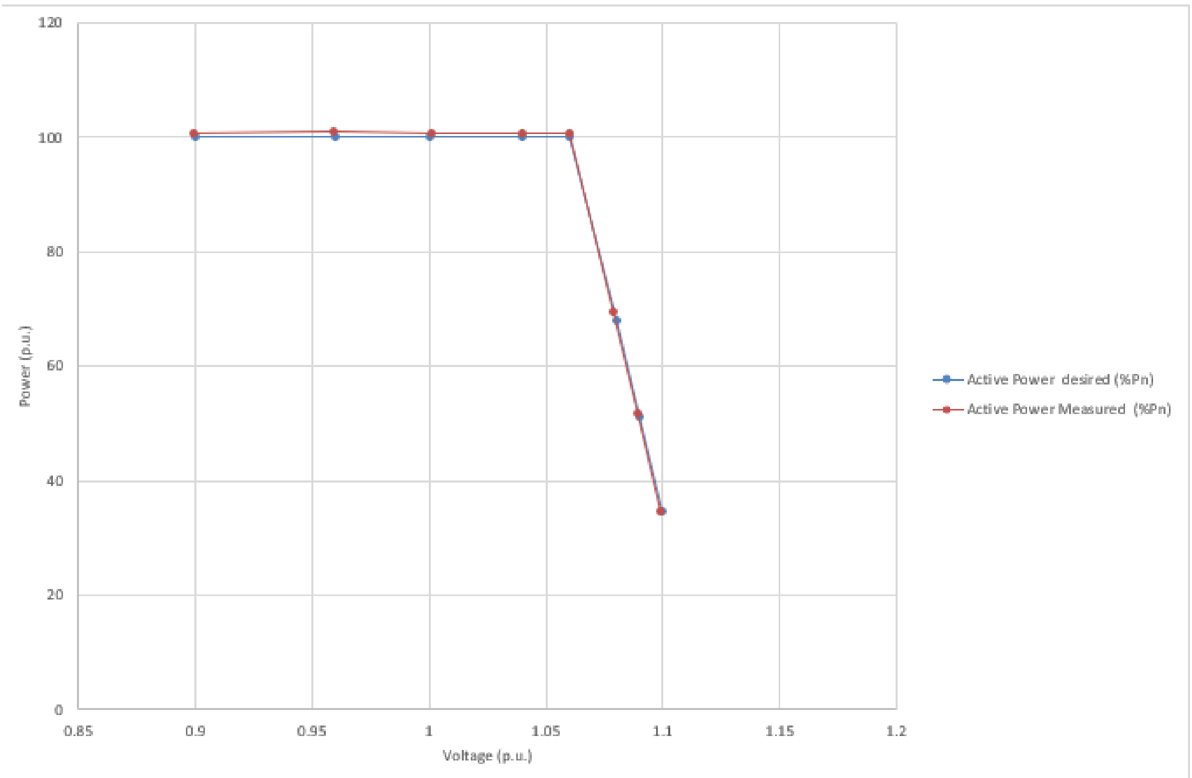


4.13.1.1.2 Test 2 (for New Zealand setting)

Voltage desired (%Un)	Voltage Measured (%Un)	Active Power desired (%Pn)	Active Power Measured (%Pn)	Active Power Deviation (%Pn)
90.0	89.9	100.0	100.8	0.8
96.0	95.9	100.0	101.0	1.0
100.0	100.1	100.0	100.7	0.7
104.0	104.0	100.0	100.8	0.8
106.0	106.0	100.0	100.8	0.8
108.0	107.9	68.0	69.6	1.6
109.0	108.9	51.3	51.9	0.6
110.0	109.9	34.5	34.5	0.0

Volt – Watt (Test 2)





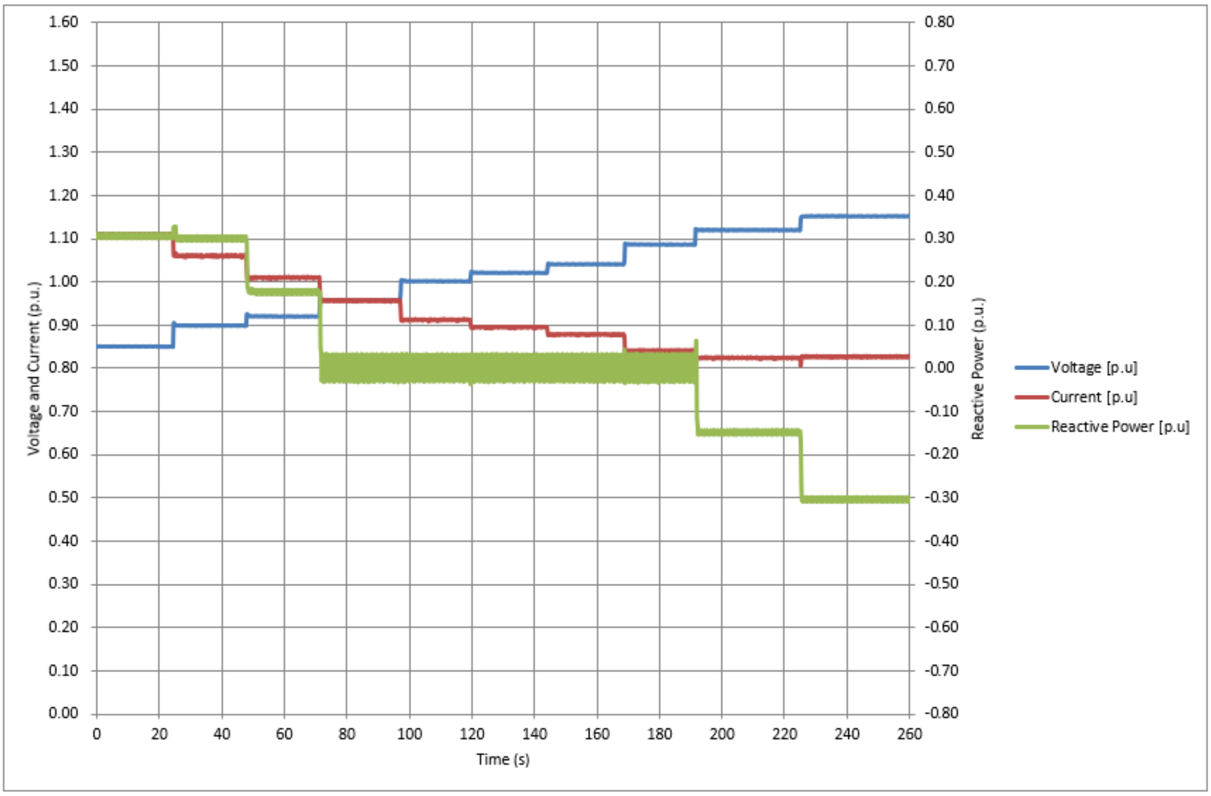
4.13.1.2 Volt –Var Response Mode

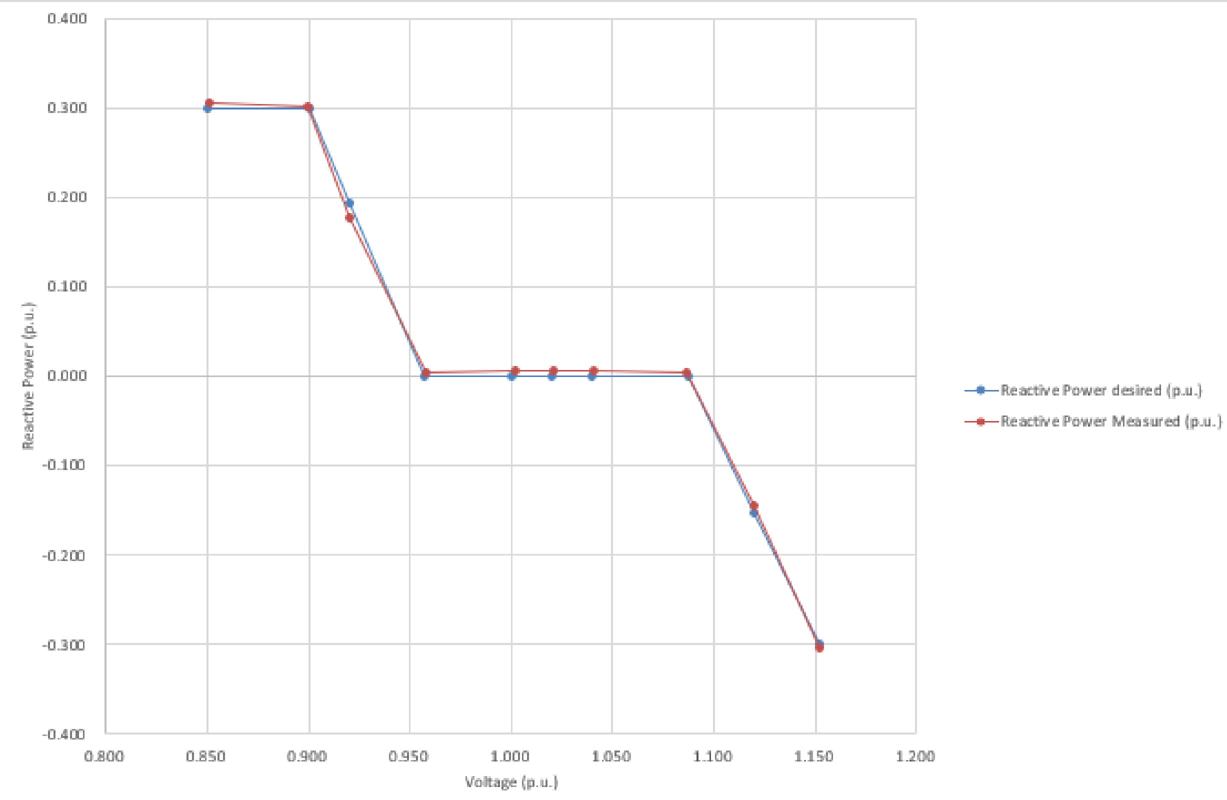
Volt – Var Response Mode has been measured according to Clause 6.3.2.3 of the standard, at the required voltage and VAr points of operation. Only Australia setting was tested for this test.

The default VAr level (30% lagging/leading) has been tested as following:

Q = 30 % Sn				
Voltage Desired (%Un)	**Voltage Measured (%Un)**	**Reactive Power desired (%Sn)**	**Reactive Power Measured (%Sn)**	**Reactive Power Deviation (%Sn)**
85.0	85.1	30.0	30.6	0.6
90.0	89.9	30.0	30.2	0.2
92.0	92.0	19.4	17.8	-0.2
95.7	95.8	0.0	0.5	0.5
100.0	100.2	0.0	0.7	0.7
102.0	102.1	0.0	0.6	0.6
104.0	104.1	0.0	0.6	0.6
108.7	108.7	0.0	0.5	0.5
112.0	112.0	-15.2	-14.5	0.7
115.2	115.2	-30.0	-30.3	-0.3

Volt – Var 30 % Sn





4.13.1.3 Voltage Balance Modes

The requirement of Voltage Balance Modes test has to be verified according to the clause 6.3.2.4 of the standard.

It is not applicable due to the inverter doesn’t provide this operation mode.

4.13.2 Fixed Power Factor Mode and Reactive Power Mode

The verification of reactive power supply capability test has been measured according to the clause 6.3.3 of the standard.

Two different tests have been evaluated:

- Test 1: Rectangular Curve Q fixed (Q=±30% Sn)
- Test 2: Triangular Curve PF fixed (PF=±0.8)

4.13.2.1 Test 1: Rectangular Curve (Q =±30%Sn)

This test verifies the capability of the inverter to provide a fixed value of reactive power. In addition, it is verified the Q control mode.

Allowed tolerance to be considered is 5%Sn when possible.

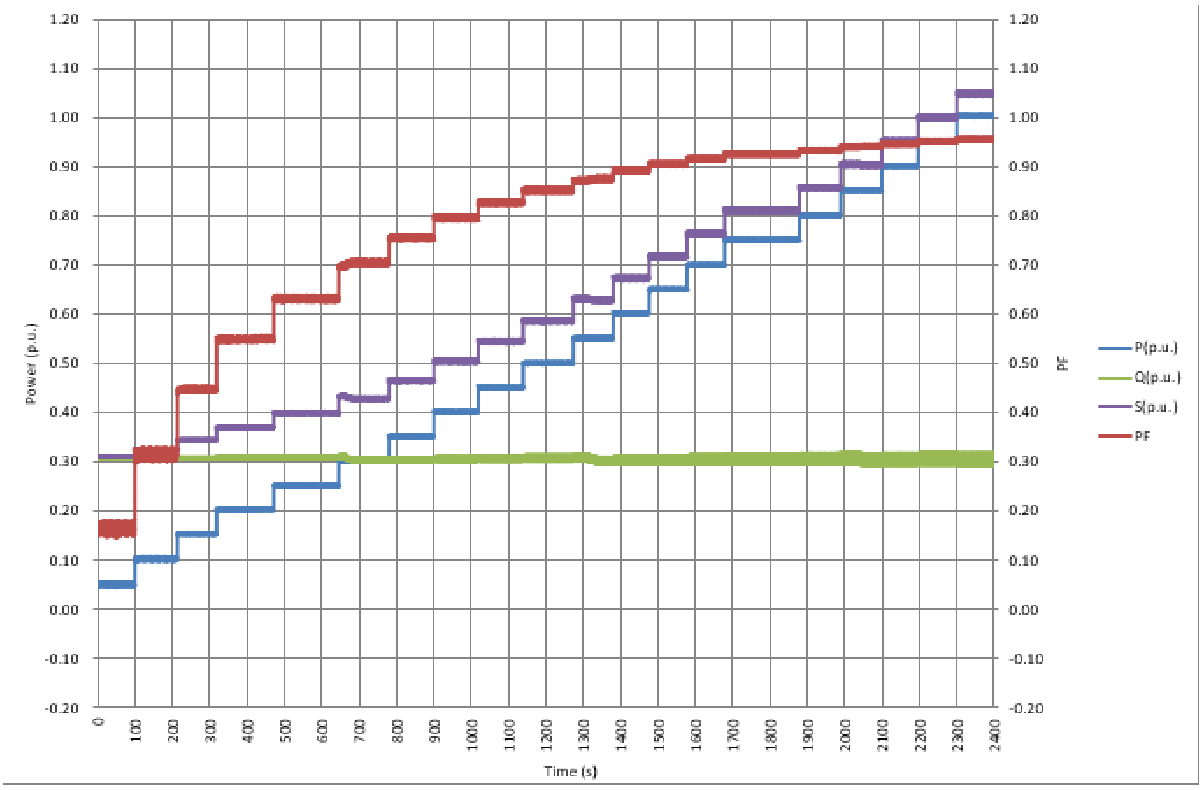
The following table shows the test results:

Rectangular Curve (Q=30.0%Sn / Inductive)					
P Desired (%Sn)	P measured (%Sn)	Q desired (%Sn)	Q measured (%Sn)	Q Deviation (%Sn)	Power Factor (cos φ)
5	5.1	30.0	30.7	0.7	0.165
10	10.2	30.0	30.8	0.8	0.315
15	15.4	30.0	30.8	0.8	0.446
20	20.3	30.0	31.0	1.0	0.548
25	25.2	30.0	31.0	1.0	0.631
30	30.2	30.0	30.5	0.5	0.703
35	35.2	30.0	30.5	0.5	0.756
40	40.2	30.0	30.6	0.6	0.796
45	45.1	30.0	30.7	0.7	0.827
50	50.1	30.0	30.8	0.8	0.852
55	55.2	30.0	30.6	0.6	0.875
60	60.2	30.0	30.4	0.4	0.893
65	65.1	30.0	30.5	0.5	0.906
70	70.1	30.0	30.6	0.6	0.917
75	75.2	30.0	30.6	0.6	0.926
80	80.2	30.0	30.7	0.7	0.929
85	85.2	30.0	30.6	0.6	0.941
90	90.2	30.0	30.6	0.6	0.947
95	95.2	30.0	30.6	0.6	0.952
100	100.4	30.0	30.5	0.5	0.957

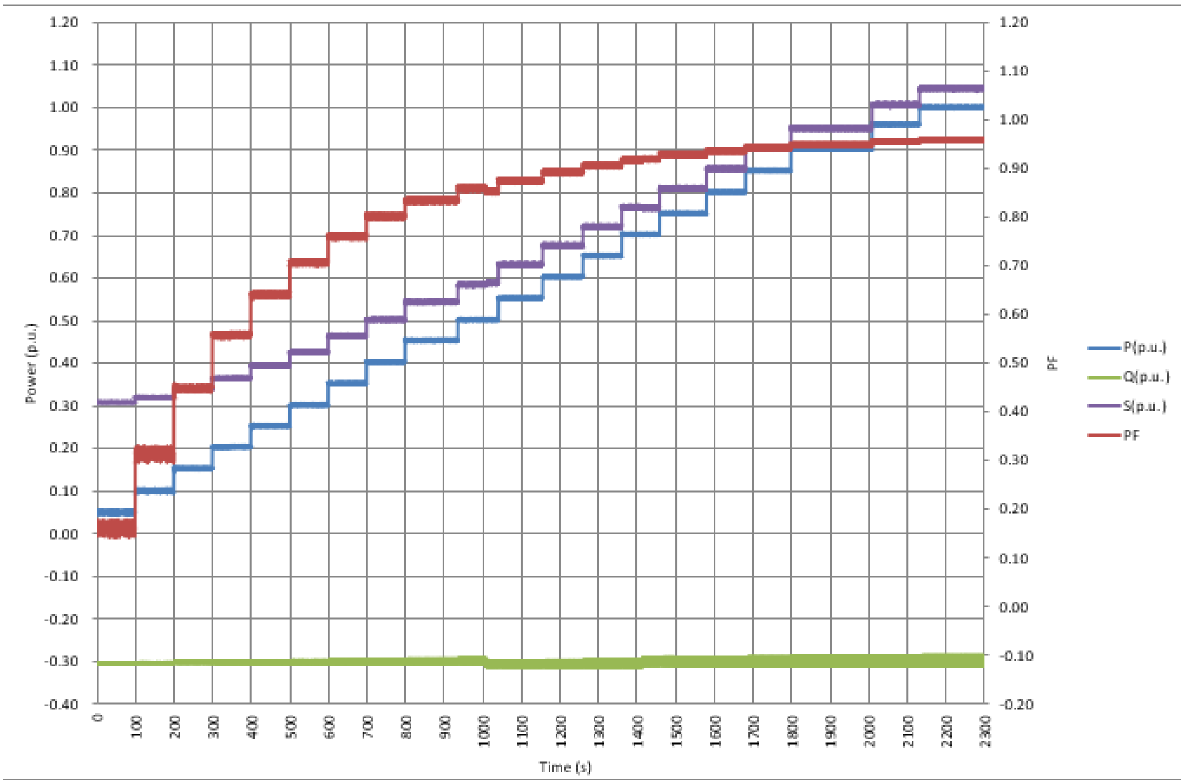
Rectangular Curve (Q=30.0%Sn / Capacitive)					
P Desired (%Sn)	**P measured (%Sn)**	**Q desired (%Sn)**	**Q measured (%Sn)**	**Q Deviation (%Sn)**	**Power Factor (cos φ)**
5	5.0	-30.0	-30.4	-0.4	0.161
10	10.1	-30.0	-30.3	-0.3	0.315
15	15.2	-30.0	-30.2	-0.2	0.450
20	20.4	-30.0	-30.2	-0.2	0.559
25	25.3	-30.0	-30.2	-0.2	0.642
30	30.2	-30.0	-30.1	-0.1	0.708
35	35.3	-30.0	-30.1	-0.1	0.761
40	40.3	-30.0	-30.0	0.0	0.802
45	45.3	-30.0	-29.9	0.1	0.834
50	50.2	-30.0	-30.1	-0.1	0.857
55	55.3	-30.0	-30.6	-0.6	0.875
60	60.3	-30.0	-30.6	-0.6	0.892
65	65.3	-30.0	-30.5	-0.5	0.906
70	70.2	-30.0	-30.2	-0.2	0.918
75	75.2	-30.0	-30.1	-0.1	0.928
80	80.2	-30.0	-30.1	-0.1	0.936
85	85.2	-30.0	-30.0	0.0	0.943
90	90.3	-30.0	-30.0	0.0	0.949
95	96.1	-30.0	-29.9	0.1	0.955
100	100.1	-30.0	-29.9	0.1	0.958

Test results are represented at diagrams below.

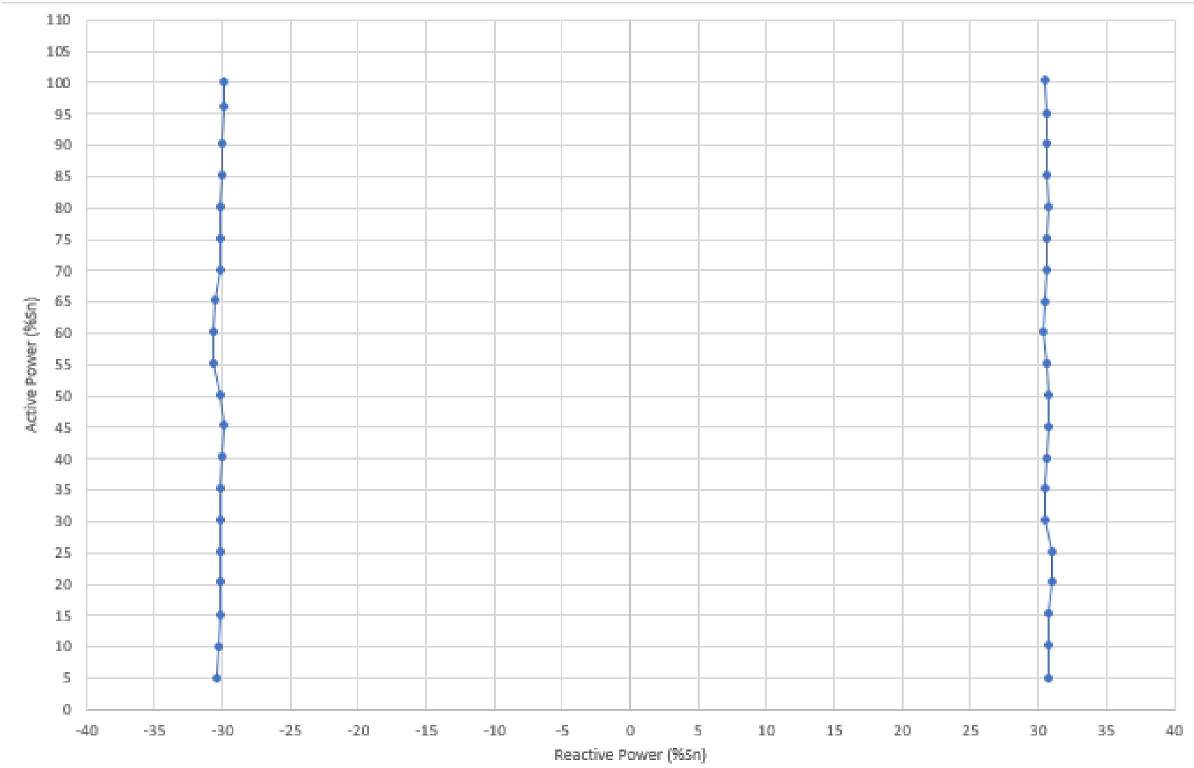
Rectangular Curve (Q=30.0%Sn / Inductive)



Rectangular Curve (Q=30.0%S_n / Capacitive)



Rectangular Curve (Capacitive vs Inductive)



4.13.2.2 Test 2: Triangular Curve (PF=±0.8)

This test verifies the capability of the inverter to provide a fixed value of power factor. In addition, it is verified the PF control mode.

At high active power levels, the reactive power provided by the inverter is automatically limited by the inverter in order to protect against over current.

The maximum tolerance allowed for the measured Power Factor is ± 0.01, for measurements from 25%Sn.

The following table and graphs show test results for measurements of power factor set to 0.800 inductive:

Fixed Power Factor (PF=0.800 / Inductive)					
P Desired (%Sn)	**P measured (%Sn)**	**Q measured (%Sn)**	**Power Factor desired (cos φ)**	**Power Factor measured (cos φ)**	**Power Factor Deviation (cos φ)**
5	4.8	3.5	0.800	0.811	0.011 (**)
10	9.5	6.7	0.800	0.817	0.017 (**)
15	15.0	11.3	0.800	0.800	0.000
20	20.1	15.0	0.800	0.802	0.002
25	25.2	18.9	0.800	0.801	0.001
30	30.3	22.8	0.800	0.800	0.000
35	35.1	26.5	0.800	0.799	-0.001
40	40.2	30.3	0.800	0.798	-0.002
45	45.1	34.0	0.800	0.798	-0.002
50	50.1	37.9	0.800	0.798	-0.002
55	55.2	41.7	0.800	0.798	-0.002
60	60.2	45.5	0.800	0.798	-0.002
65	65.1	49.3	0.800	0.797	-0.003
70	70.1	53.1	0.800	0.797	-0.003
75	75.1	56.9	0.800	0.797	-0.003
80	80.1	60.7	0.800	0.797	-0.003
85	85.0	64.5	0.800	0.797	-0.003
90	89.2	67.6	0.800	0.797	-0.003
95(*)	-	-	-	-	-
100(*)	-	-	-	-	-

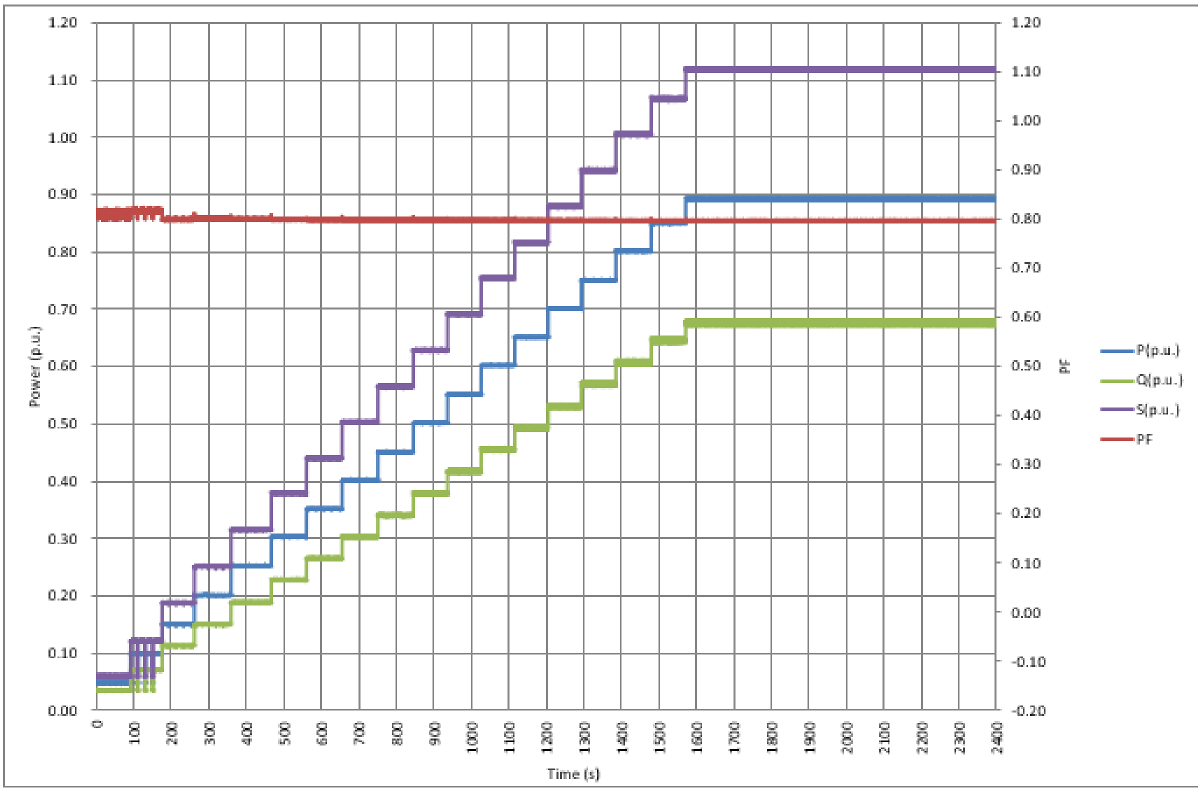
(*) It is reactive power priority in this mode. The inverter does not reach the desired active power above 89.0%Pn due to current limitation.
(**) It is allowed that he maximum tolerance for the measured Power Factor is outside ± 0.01, for measurements below 25%Sn.

The following table and graphs show test results for measurements of power factor set to 0.800 capacitive:

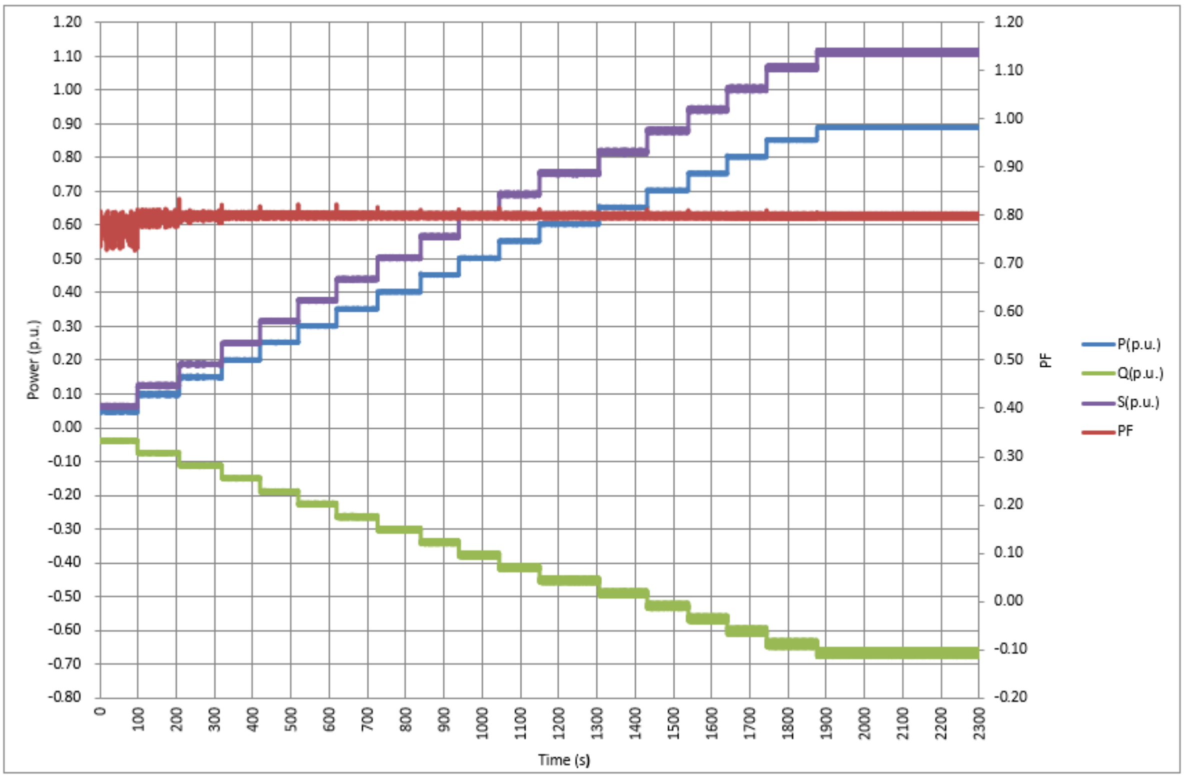
Fixed Power Factor (PF=0.800 / Capacitive)					
P Desired (%Sn)	**P measured (%Sn)**	**Q measured (%Sn)**	**Power Factor desired (cos φ)**	**Power Factor measured (cos φ)**	**Power Factor Deviation (cos φ)**
5	4.8	-3.9	0.800	0.782	-0.018 (**)
10	9.9	-7.5	0.800	0.797	-0.003
15	15.0	-11.3	0.800	0.800	0.000
20	20.1	-15.0	0.800	0.801	0.001
25	25.3	-19.0	0.800	0.801	0.001
30	30.2	-22.6	0.800	0.800	0.000
35	35.2	-26.4	0.800	0.800	0.000
40	40.3	-30.2	0.800	0.800	0.000
45	45.3	-34.0	0.800	0.800	0.000
50	50.3	-37.7	0.800	0.800	0.000
55	55.3	-41.5	0.800	0.800	0.000
60	60.3	-45.3	0.800	0.800	0.000
65	65.3	-49.1	0.800	0.800	0.000
70	70.3	-52.8	0.800	0.800	0.000
75	75.3	-56.6	0.800	0.800	0.000
80	80.3	-60.3	0.800	0.800	0.000
85	85.3	-64.1	0.800	0.799	-0.001
90	89.0	-66.8	0.800	0.800	0.000
95(*)	-	-	-	-	-
100(*)	-	-	-	-	-

(*) It is reactive power priority in this mode. The inverter does not reach the desired active power above 89.0%Pn due to current limitation.
(**) It is allowed that he maximum tolerance for the measured Power Factor is outside ± 0.01, for measurements below 25%Sn.

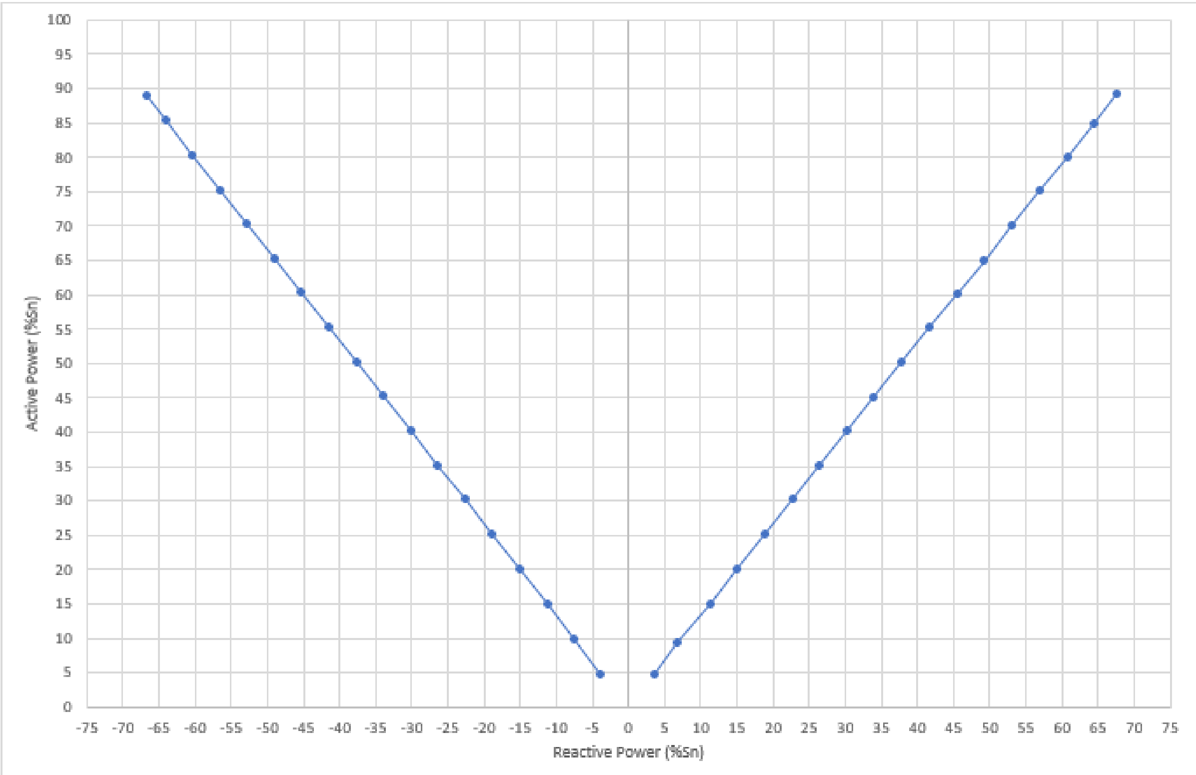
Triangular Curve (PF=0.80 / Inductive)



Triangular Curve (PF=0.8 / Capacitive)

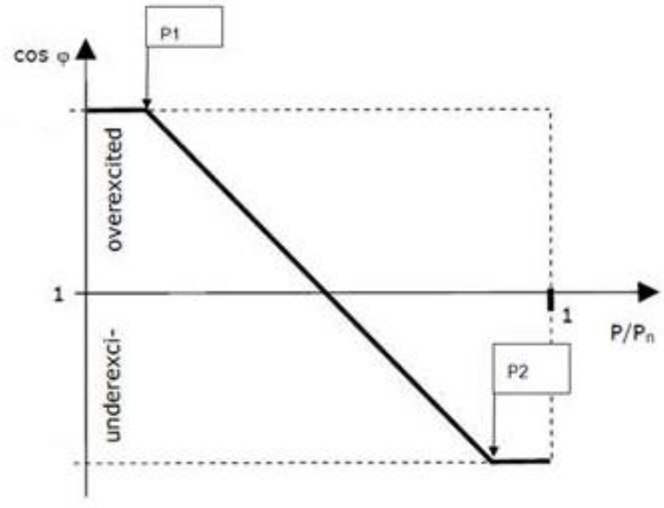


Triangular Curve (Inductive vs Capacitive)



4.13.3 Characteristics Power Factor Curve for Cos ϕ (Power Response)

The Characteristic Power Factor Curve for cos ϕ (Power response) has been measured according to the Clause 6.3.4 of the standard. Three tests have been done to verify an adjustable curve from PF inductive to PF capacitive.



These tests have been performed as detailed in following table:

Test Nº	Point P1		Point P2	
	Active Power (%Sn)	Power Factor	Active Power (%Sn)	Power Factor
1	20%	0.95	90%	-0.95
2	20%	0.90	90%	-0.90
3	20%	0.95	80%	-0.95

For all tests above detailed, the unity power factor is reached at 50%Pn.

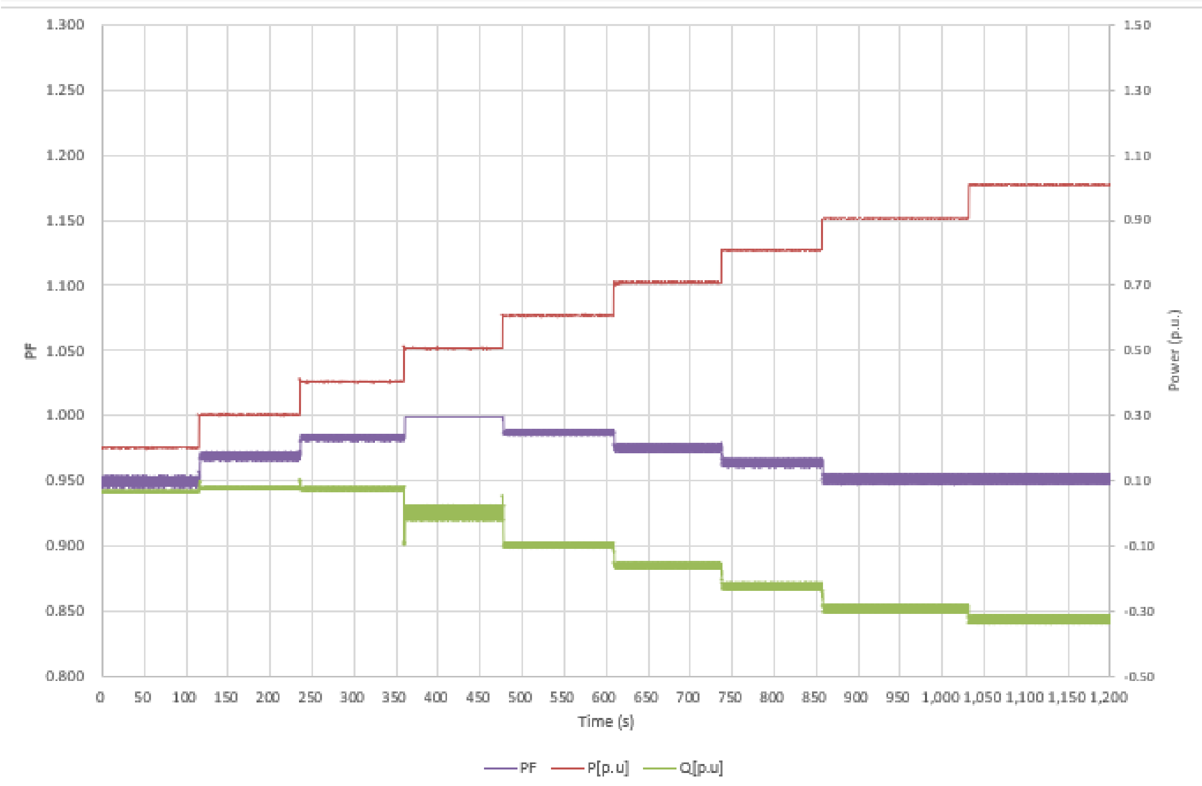
There is allowed a maximum tolerance for power factor measurement inside ±0.01.

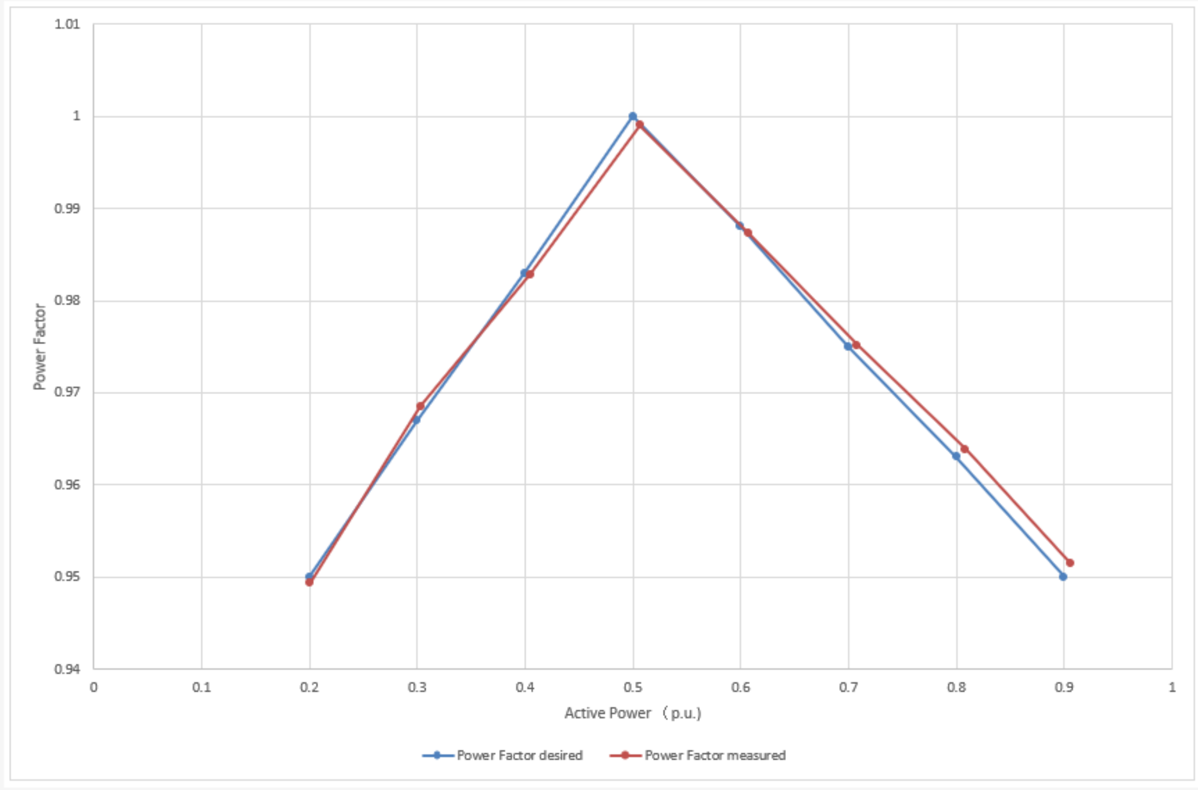
4.13.3.1 Test 1

In this test it is verified that the power factor varies linearly from PF = 0.95 (inductive) at 20%Pn, PF = 1 at 50%Pn, PF = 0.95 (capacitive) at 90%Pn. The following table shows the obtained test results:

P Desired (%Sn)	P measured (%Sn)	Q measured (%Sn)	Power Factor desired (cos φ)	Power Factor measured (cos φ)	Power Factor Deviation (cos φ)
20	20.1	6.7	0.950	0.949	-0.001
30	30.3	7.8	0.967	0.969	0.002
40	40.5	7.6	0.983	0.983	0.000
50	50.7	0.4	1.000	0.999	-0.001
60	60.8	-9.7	0.988	0.987	-0.001
70	70.8	-16.1	0.975	0.975	0.000
80	80.9	-22.3	0.963	0.964	0.001
90	90.6	-29.3	0.950	0.951	0.001

Characteristic curve Cos φ (P) Test 1



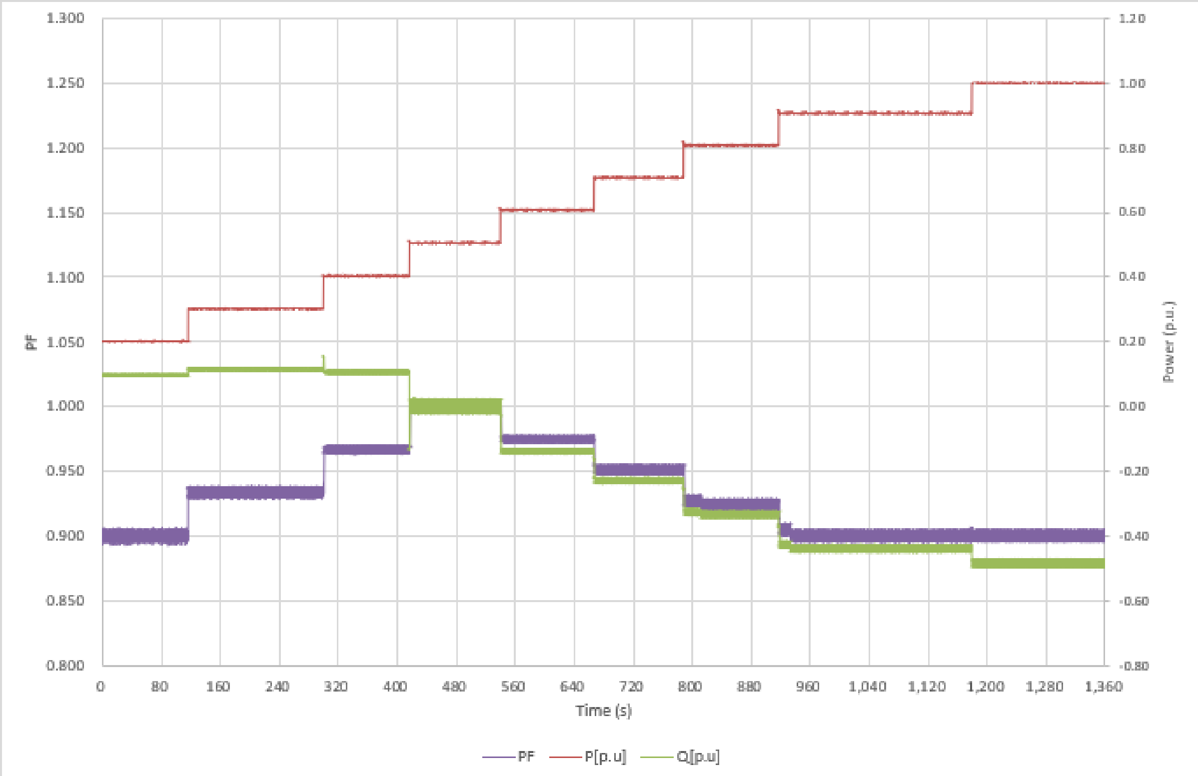


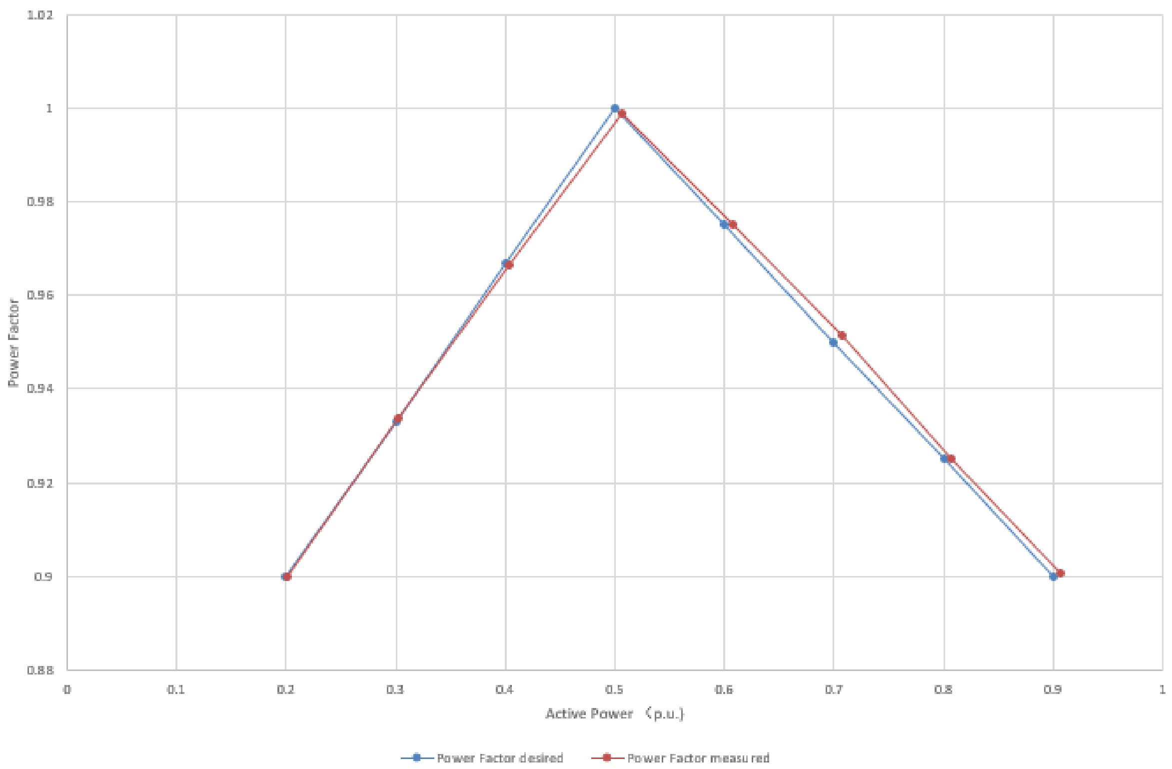
4.13.3.2 Test 2

In this test it is verified that the power factor varies linearly from PF = 0.90 (inductive) at 20%Pn, PF = 1 at 50%Pn, PF = 0.90 (capacitive) at 90%Pn. The following table shows the obtained test results:

P Desired (%Sn)	P measured (%Sn)	Q measured (%Sn)	Power Factor desired (cos φ)	Power Factor measured (cos φ)	Power Factor Deviation (cos φ)
20	20.1	9.7	0.900	0.900	0.000
30	30.2	11.6	0.933	0.934	0.001
40	40.4	10.7	0.967	0.966	-0.001
50	50.6	-0.1	1.000	0.999	-0.001
60	60.7	-13.7	0.975	0.975	0.000
70	70.7	-22.9	0.950	0.951	0.001
80	80.7	-33.1	0.925	0.925	0.000
90	90.7	-43.8	0.900	0.901	0.001

Characteristic curve Cos φ (P) Test 2



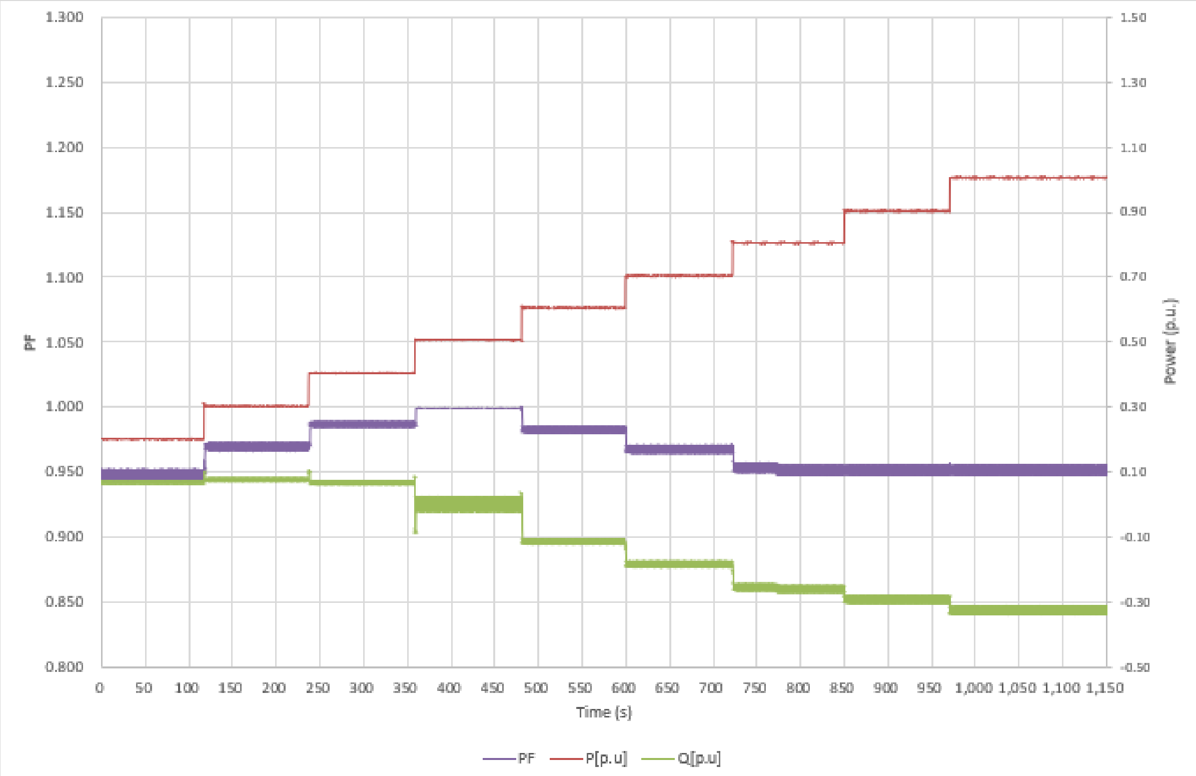


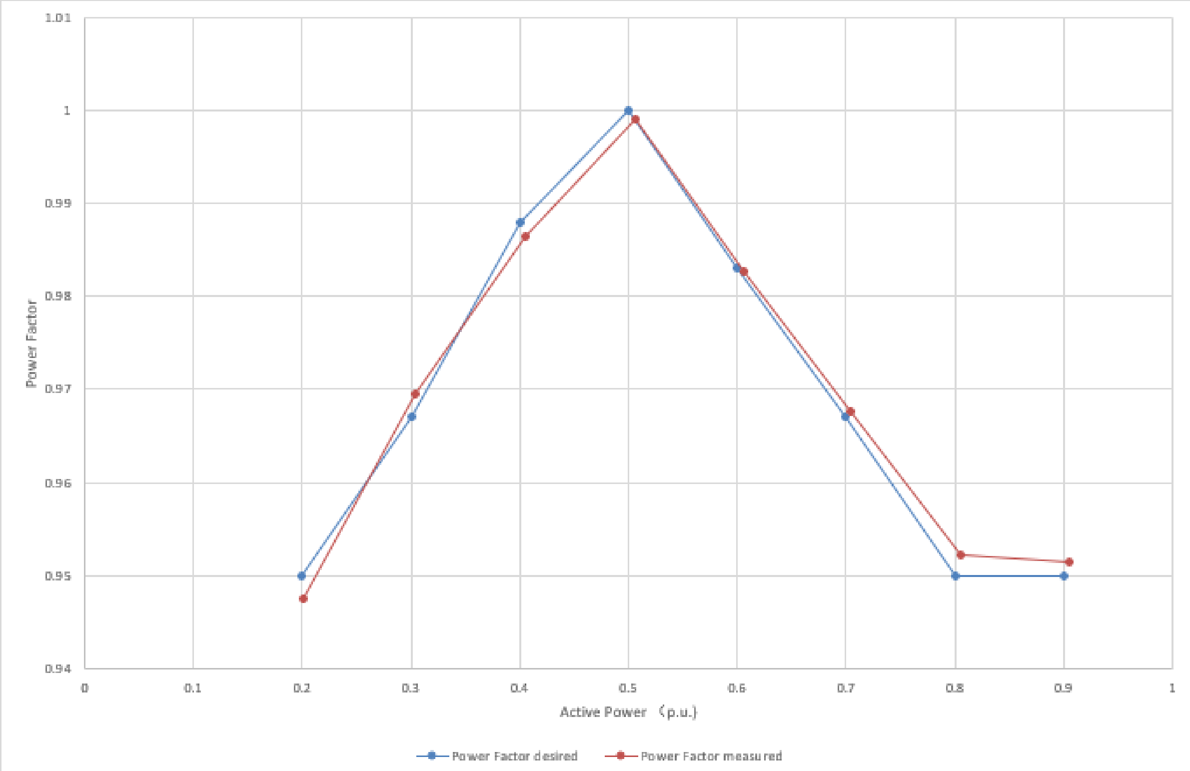
4.13.3.3 Test 3

In this test it is verified that the power factor vary linearly from PF = 0.95 (inductive) at 20%Pn to PF = 0.95 (capacitive) at 80%Pn. The following table shows the obtained test results:

P Desired (%Sn)	P measured (%Sn)	Q measured (%Sn)	Power Factor desired (cos φ)	Power Factor measured (cos φ)	Power Factor Deviation (cos φ)
20	20.1	6.8	0.950	0.948	-0.002
30	30.3	7.7	0.967	0.969	0.002
40	40.5	6.7	0.988	0.986	-0.002
50	50.6	0.1	1.000	0.999	-0.001
60	60.7	-11.4	0.983	0.983	0.000
70	70.4	-18.4	0.967	0.968	0.001
80	80.5	-25.8	0.950	0.952	0.002
90	90.4	-29.3	0.950	0.951	0.001

Characteristic curve Cos φ (P) Test 3

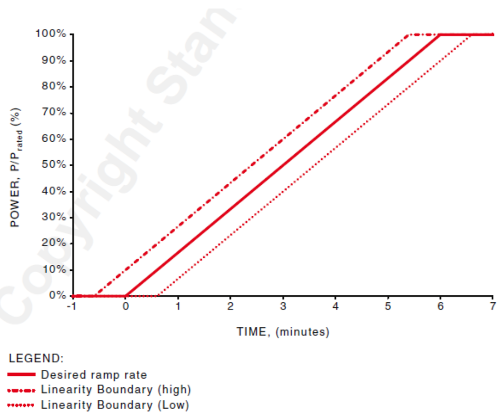




4.13.4 Power rate limit

According to the Clause 6.3.5 of the standard, the equipment shall have the capability to gradually increase and decrease its output power when requested.

The maximum NL (Nonlinearity) shall be less 10% according to standard.

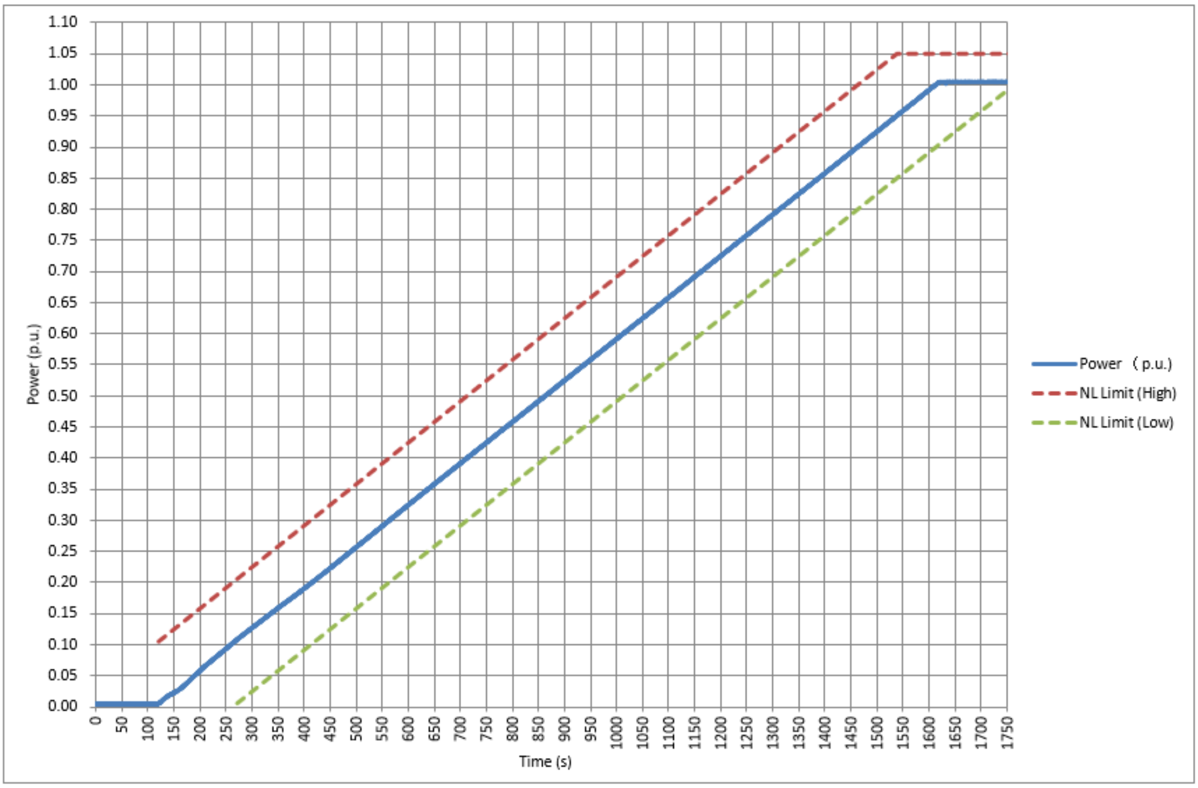


Gradients have ability to set from 4%Pn/min to 100%Pn/min by the control system of the inverter. Test results are offered in the table and pictures below:

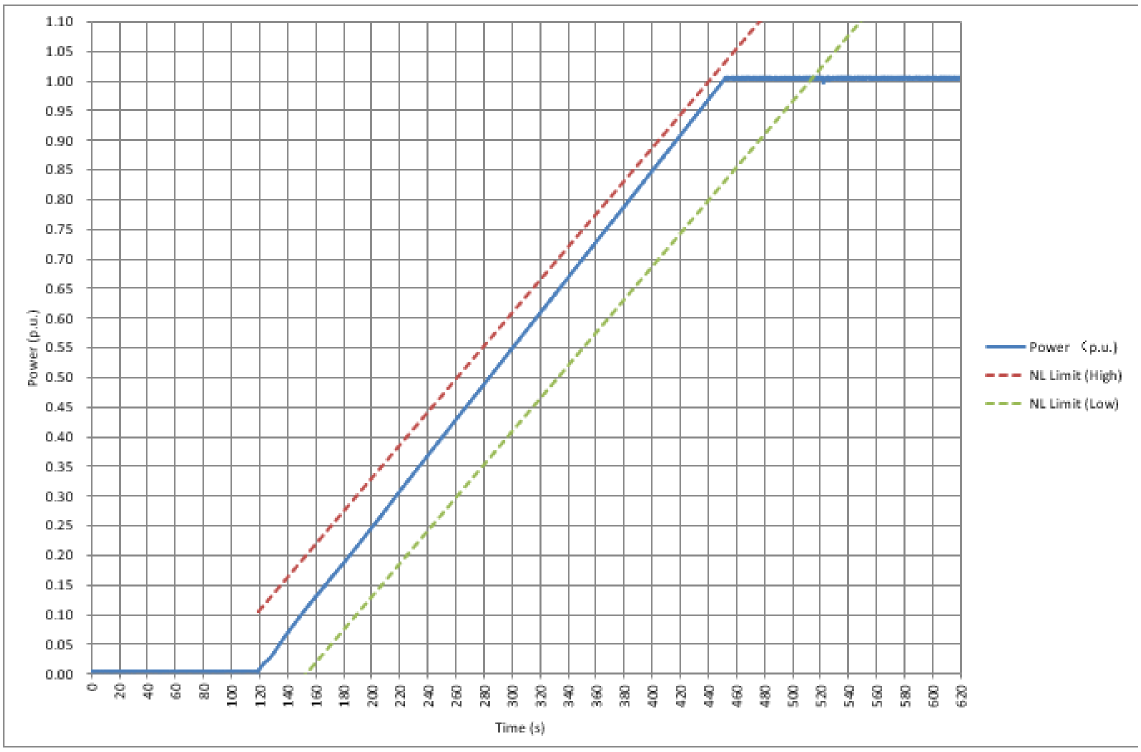
4.13.4.1 Test 1 Soft ramp up after connect or reconnect

Increase of Active Power			
Gradient (ΔP) desired (%P_n/min)	**Nominal Ramp Time (s)**	**Gradient measured (%P_n/min)**	**Measured Ramp time (s)**
4%	1500	4.0%	1491.2
16.7%	360	18.0%	331.6
100%	60	102.0%	58.6

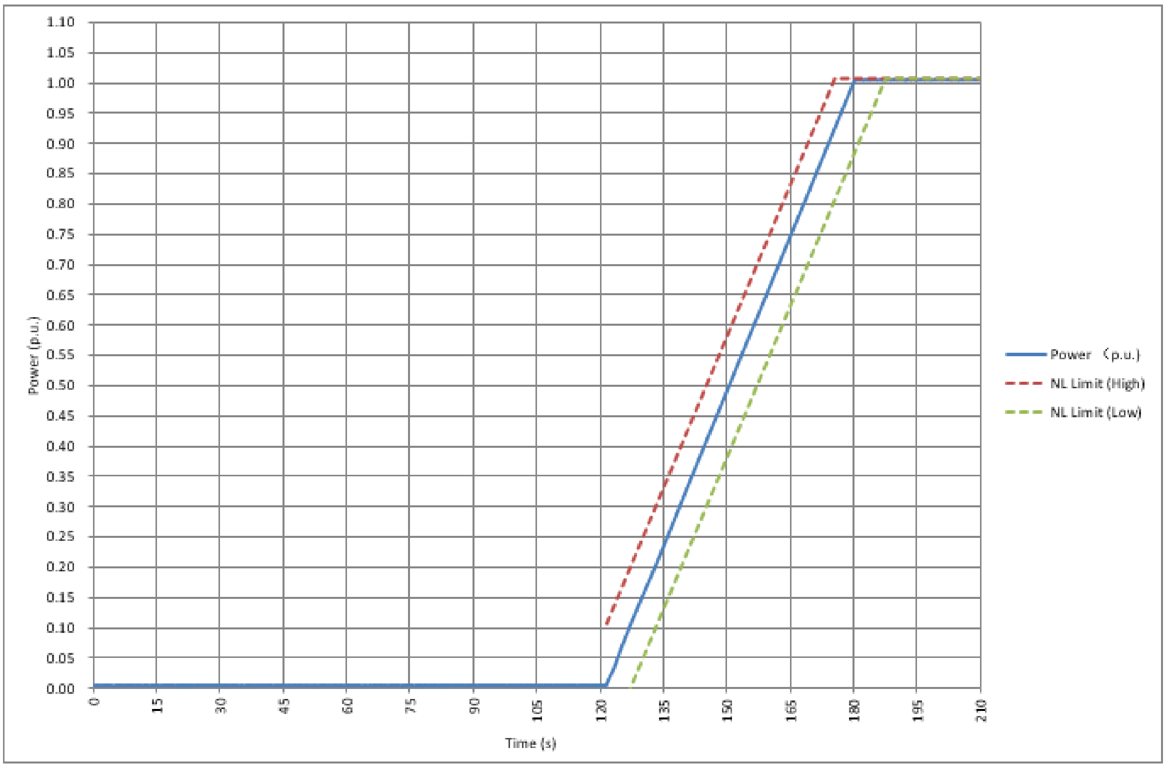
Increase of Active Power with 4%Pn/min



Increase of Active Power with 16.7%Pn/min

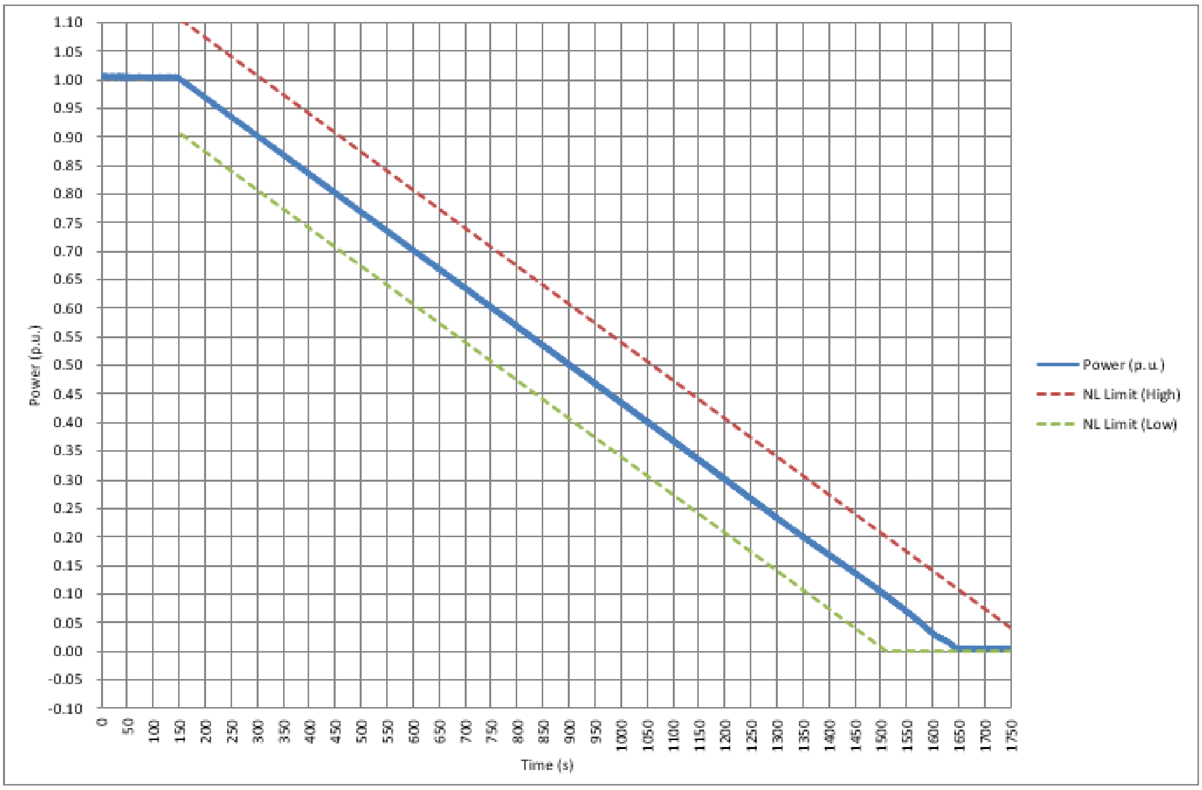


Increase of Active Power with 100%Pn/min

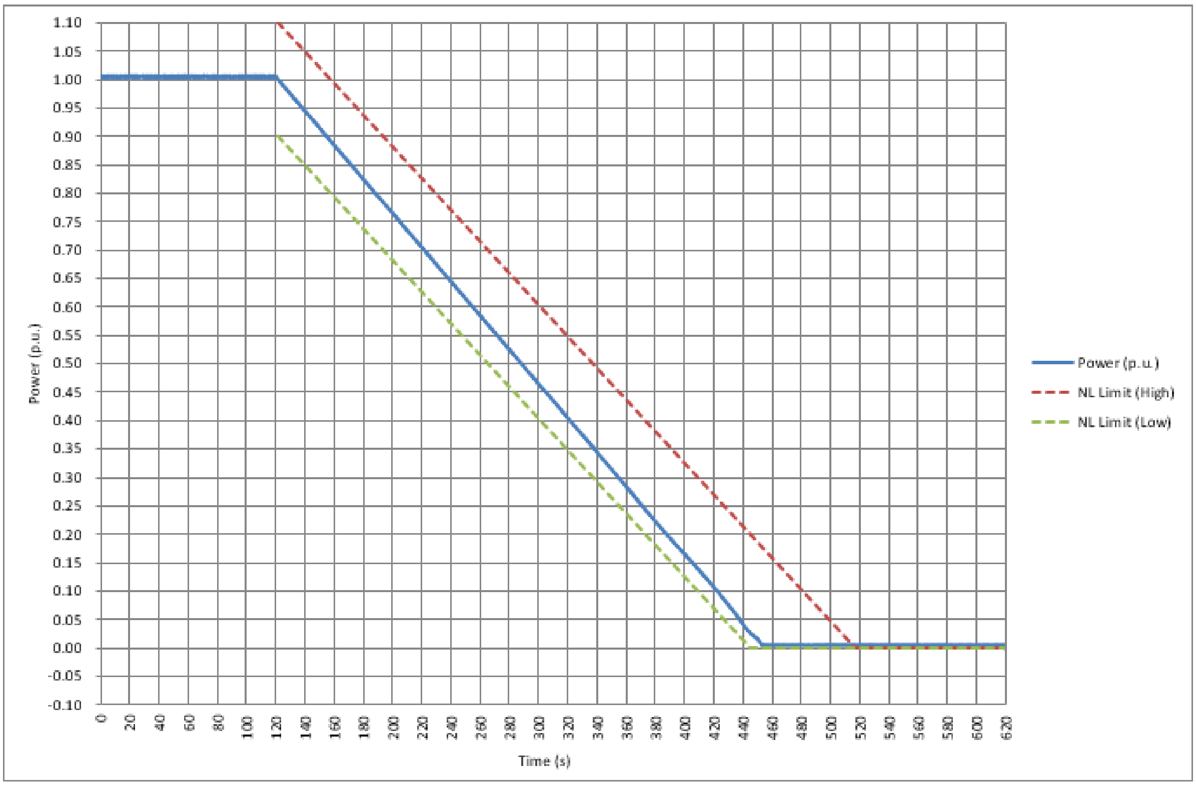


Decrease of Active Power			
Gradient (ΔP) desired (%P_n/min)	Nominal Ramp Time (s)	Gradient measured (%P_n/min)	Measured Ramp time (s)
4%	1500	4.0%	1490.4
16.7%	360	18.0%	330.2
100%	60	102.7%	58.2

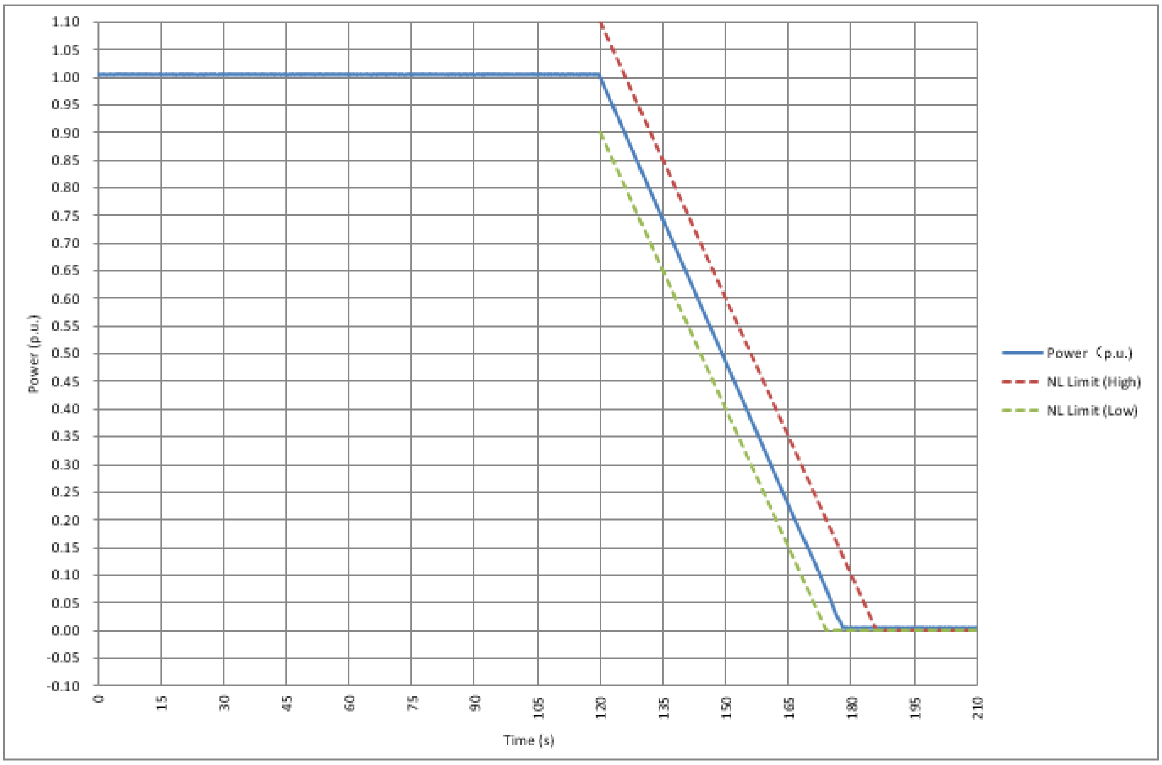
Decrease of Active Power with 4%Pn/min



Decrease of Active Power with 16.7%Pn/min



Decrease of Active Power with 100%Pn/min

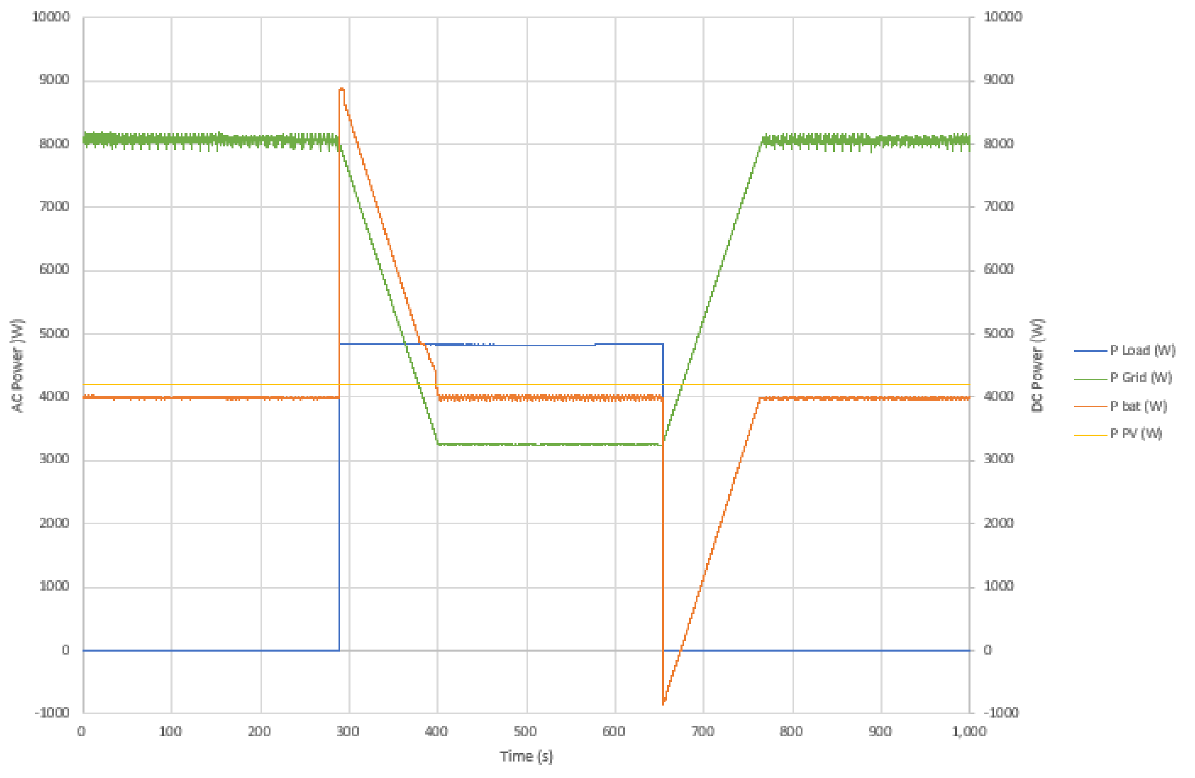


4.13.4.2 Test 2 Changes in a.c. operation and control

Test results are offered in the table and pictures below:

Increase of Active Power		Decrease of Active Power	
Gradient (ΔP) desired ($\%P_n$/min)	Gradient measured ($\%P_n$/min)	Gradient (ΔP) desired ($\%P_n$/min)	Gradient measured ($\%P_n$/min)
16.7%	17.1%	16.7%	17.1%

Test results - 16.7%Pn/min

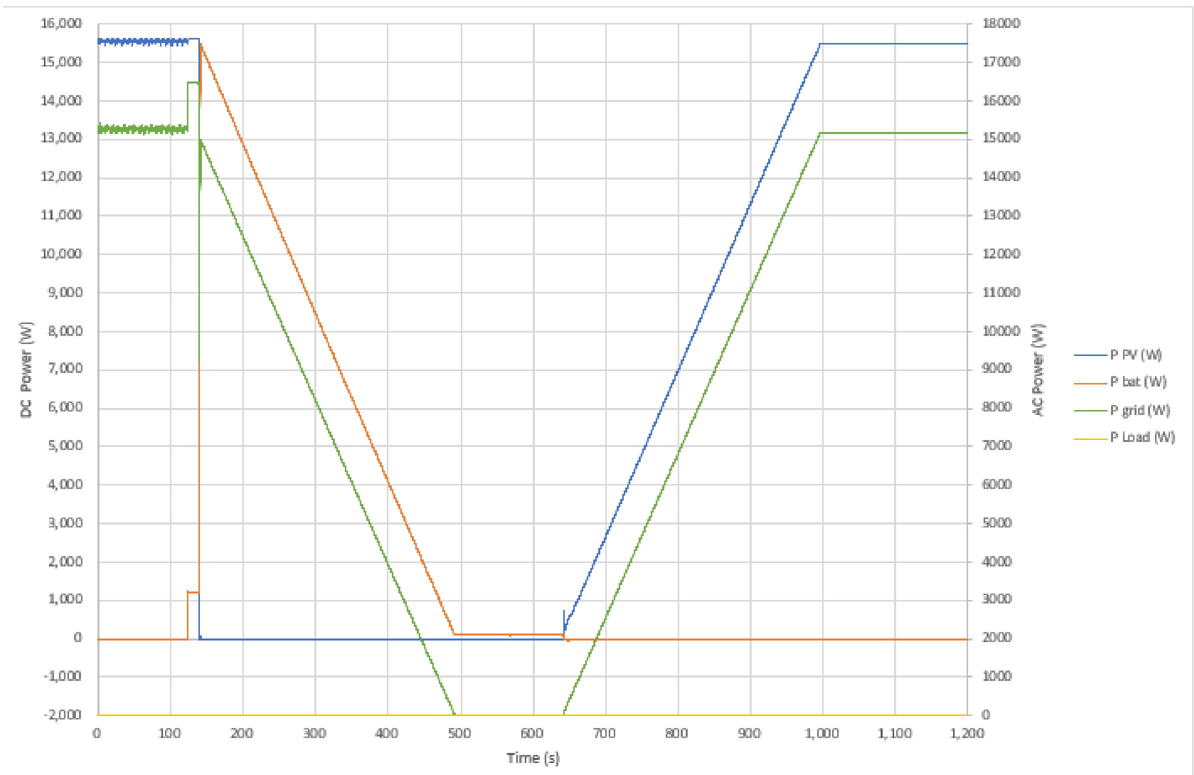


4.13.4.3 Test 3 Changes in energy source operation

Test results are offered in the table and pictures below:

Increase of Active Power		Decrease of Active Power	
Gradient (ΔP) desired ($\%P_n$/min)	Gradient measured ($\%P_n$/min)	Gradient (ΔP) desired ($\%P_n$/min)	Gradient measured ($\%P_n$/min)
16.7%	17.1%	16.7%	17.1%

Test results - 16.7%Pn/min



Note: When the PV power is suddenly decreased, the battery will start to output power and let the grid output power decreased with the desired gradient. When the PV power is suddenly increased, the inverter will limit the input power to increase grid output power with the desired gradient.

4.14 MULTIPLE MODE INVERTER OPERATION

The inverter power quality response modes tests have been measured according to Clause 6.4 of the standard.

According to the Electrical connections pictures in the user manual, the inverter can work in both grid-connected mode and standalone mode. The neutral conductor keeps on when the inverter changes from grid connect to standalone.

The following operating modes are evaluated:

- Sinusoidal output in stand-alone mode
- Volt－watt response mode for charging of energy storage

Test results are offered in the following pages:

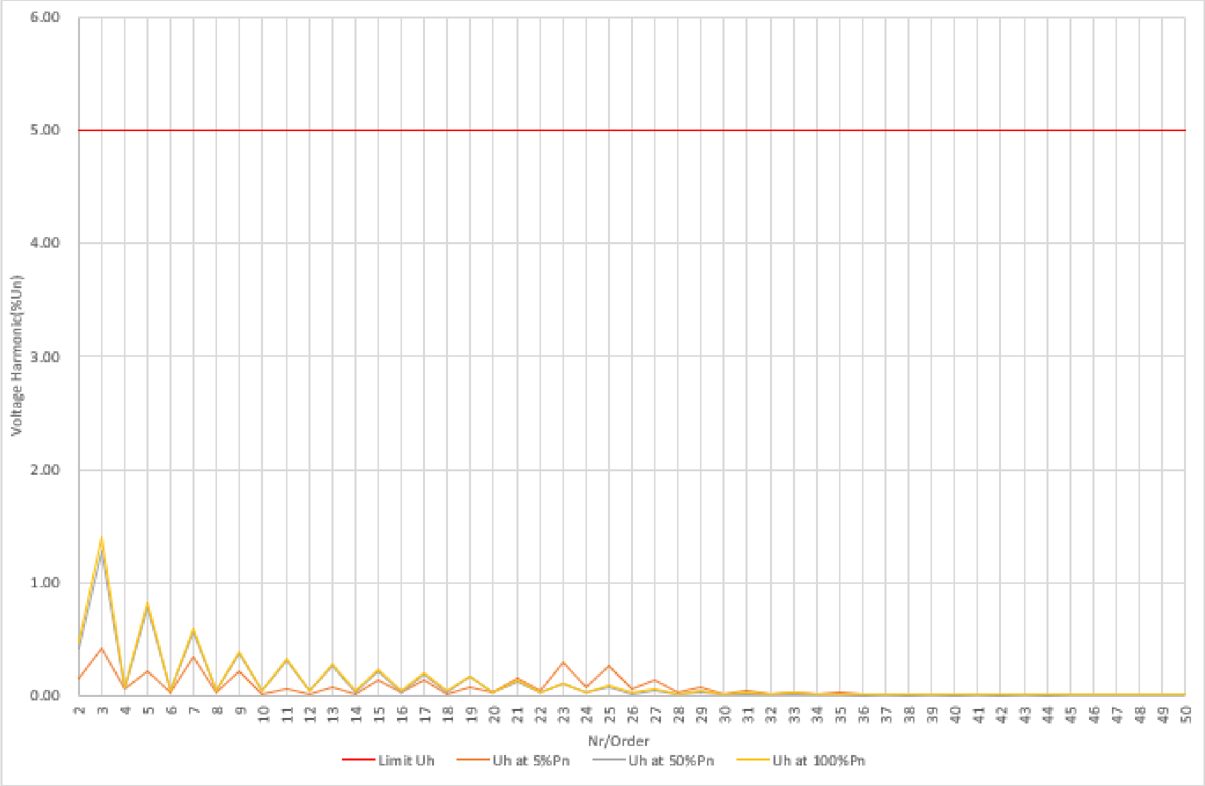
4.14.1 Sinusoidal output in stand-alone mode

Volt response modes tests have been measured according to Clause 6.4.2 of the standard.

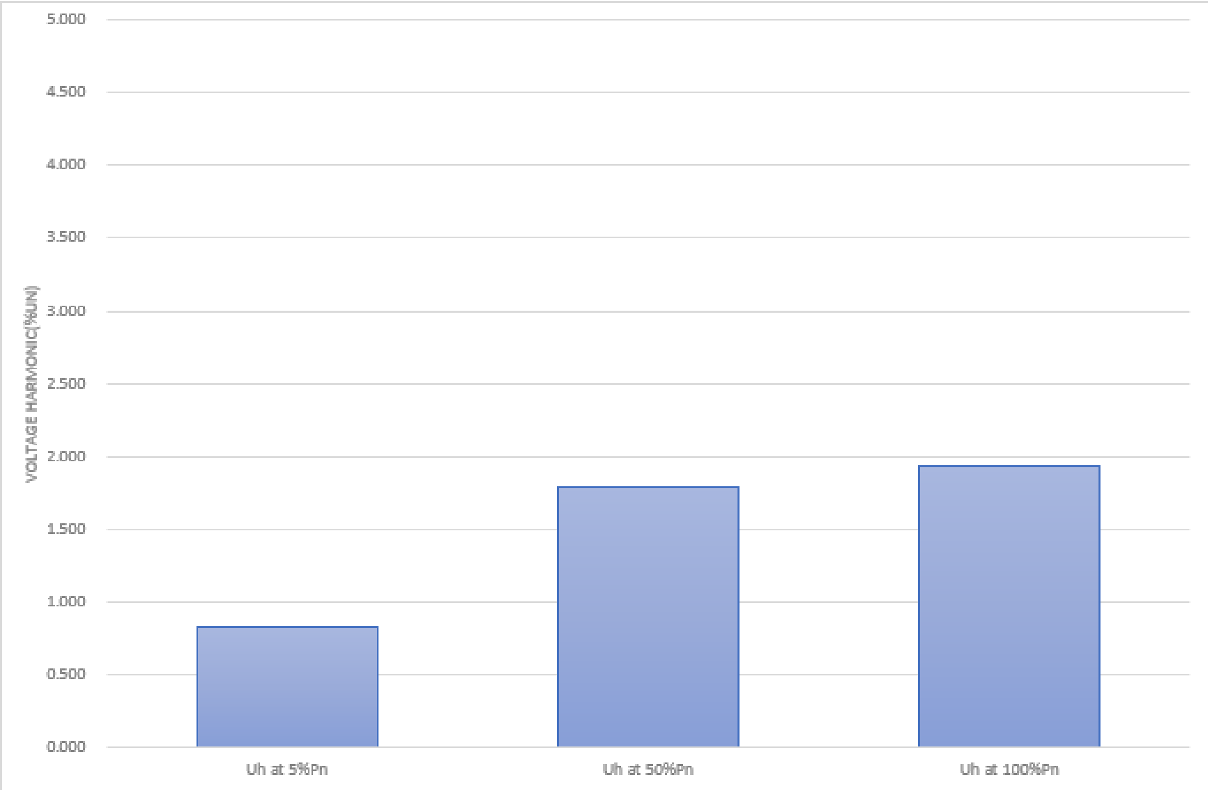
Voltage Harmonics				
Nr/Order	Limit U_h (%fundamental)	U_h at 5%Pn (%fundamental)	U_h at 50%Pn (%fundamental)	U_h at 100%Pn (%fundamental)
2	5.000	0.149	0.423	0.480
3	5.000	0.420	1.274	1.401
4	5.000	0.056	0.058	0.071
5	5.000	0.221	0.782	0.826
6	5.000	0.031	0.052	0.053
7	5.000	0.341	0.564	0.589
8	5.000	0.032	0.040	0.040
9	5.000	0.212	0.372	0.390
10	5.000	0.022	0.039	0.042
11	5.000	0.065	0.309	0.327
12	5.000	0.014	0.040	0.040
13	5.000	0.072	0.263	0.278
14	5.000	0.023	0.038	0.040
15	5.000	0.140	0.212	0.226
16	5.000	0.029	0.037	0.039
17	5.000	0.135	0.189	0.198
18	5.000	0.020	0.038	0.039
19	5.000	0.082	0.167	0.173
20	5.000	0.024	0.036	0.037
21	5.000	0.163	0.132	0.138
22	5.000	0.052	0.032	0.033
23	5.000	0.288	0.106	0.113
24	5.000	0.074	0.028	0.030
25	5.000	0.270	0.077	0.089
26	5.000	0.056	0.021	0.025
27	5.000	0.133	0.044	0.063
28	5.000	0.032	0.015	0.021
29	5.000	0.079	0.028	0.047
30	5.000	0.020	0.011	0.017
31	5.000	0.046	0.018	0.035
32	5.000	0.017	0.009	0.014
33	5.000	0.034	0.012	0.025
34	5.000	0.015	0.008	0.012
35	5.000	0.023	0.009	0.020

Voltage Harmonics				
Nr/Order	Limit U_h (%fundamental)	U_h at 5%Pn (%fundamental)	U_h at 50%Pn (%fundamental)	U_h at 100%Pn (%fundamental)
36	5.000	0.010	0.008	0.011
37	5.000	0.015	0.008	0.016
38	5.000	0.010	0.007	0.010
39	5.000	0.011	0.008	0.013
40	5.000	0.009	0.007	0.009
41	5.000	0.009	0.008	0.011
42	5.000	0.008	0.008	0.009
43	5.000	0.008	0.008	0.010
44	5.000	0.009	0.008	0.009
45	5.000	0.010	0.008	0.009
46	5.000	0.009	0.008	0.008
47	5.000	0.009	0.008	0.009
48	5.000	0.009	0.008	0.008
49	5.000	0.010	0.008	0.008
50	5.000	0.010	0.008	0.008
THD(%U_n)	5.000	0.834	1.789	1.937

Voltage Harmonics

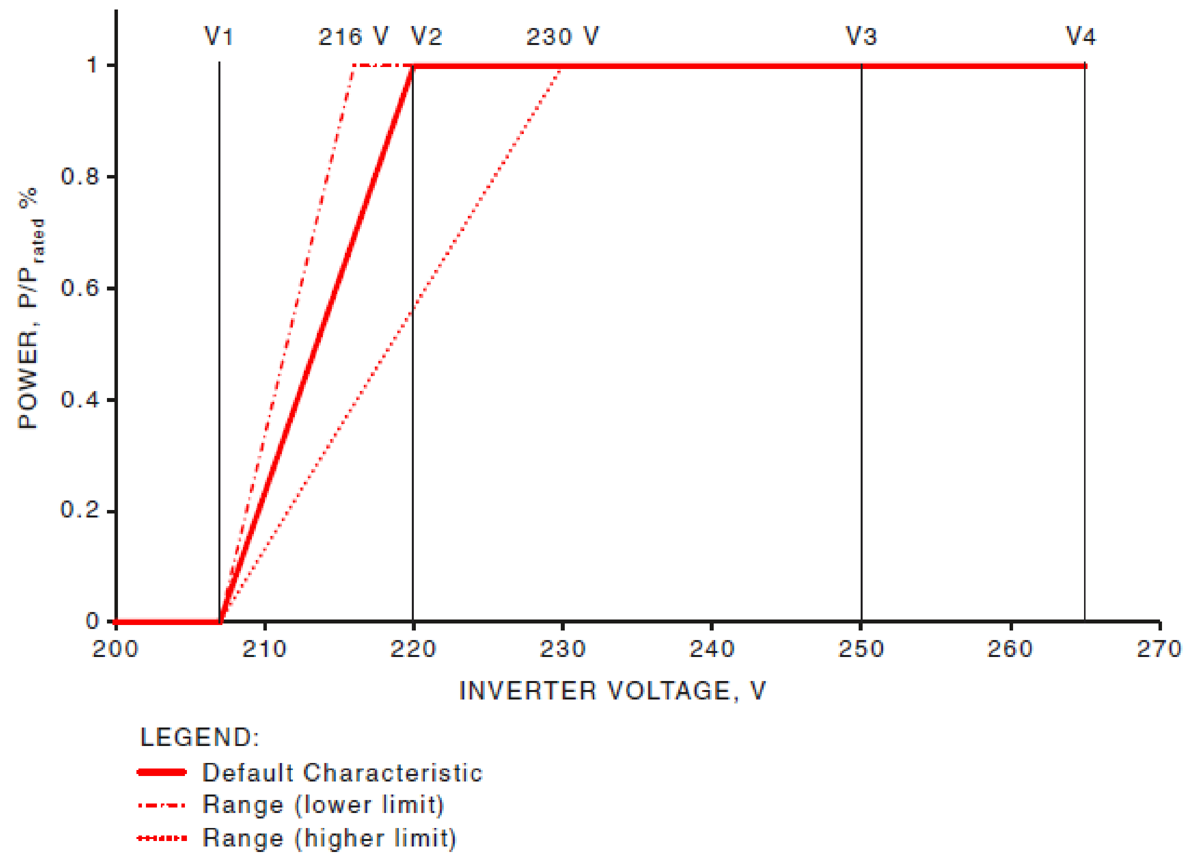


Voltage THD



4.14.2 Volt‑watt response mode for charging of energy storage

Volt response modes tests have been measured according to Clause 6.4.3 of the standard.



Two different tests have been performed to verify that the inverter volt-watt response is in accordance with the standard. These two curves tested prove also that volt-watt control function is configurable to different curves:

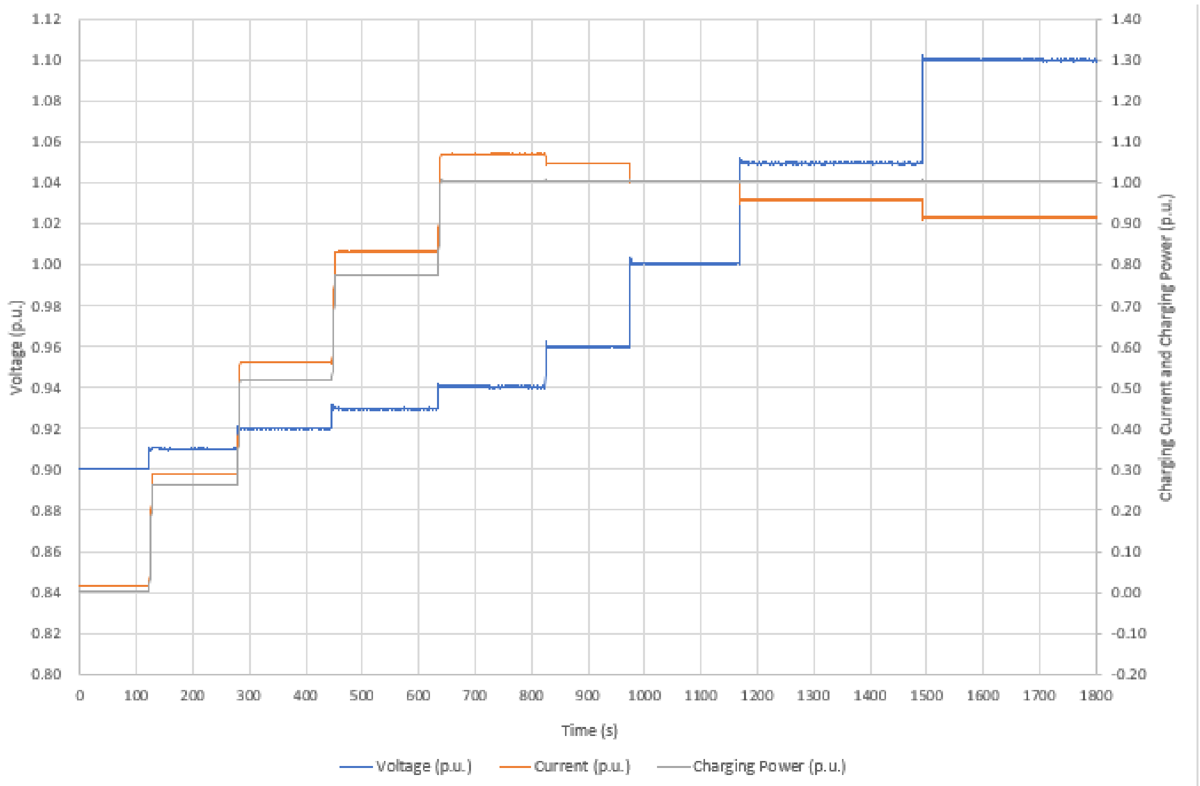
The setting values for voltage and power in the inverter have been the following:

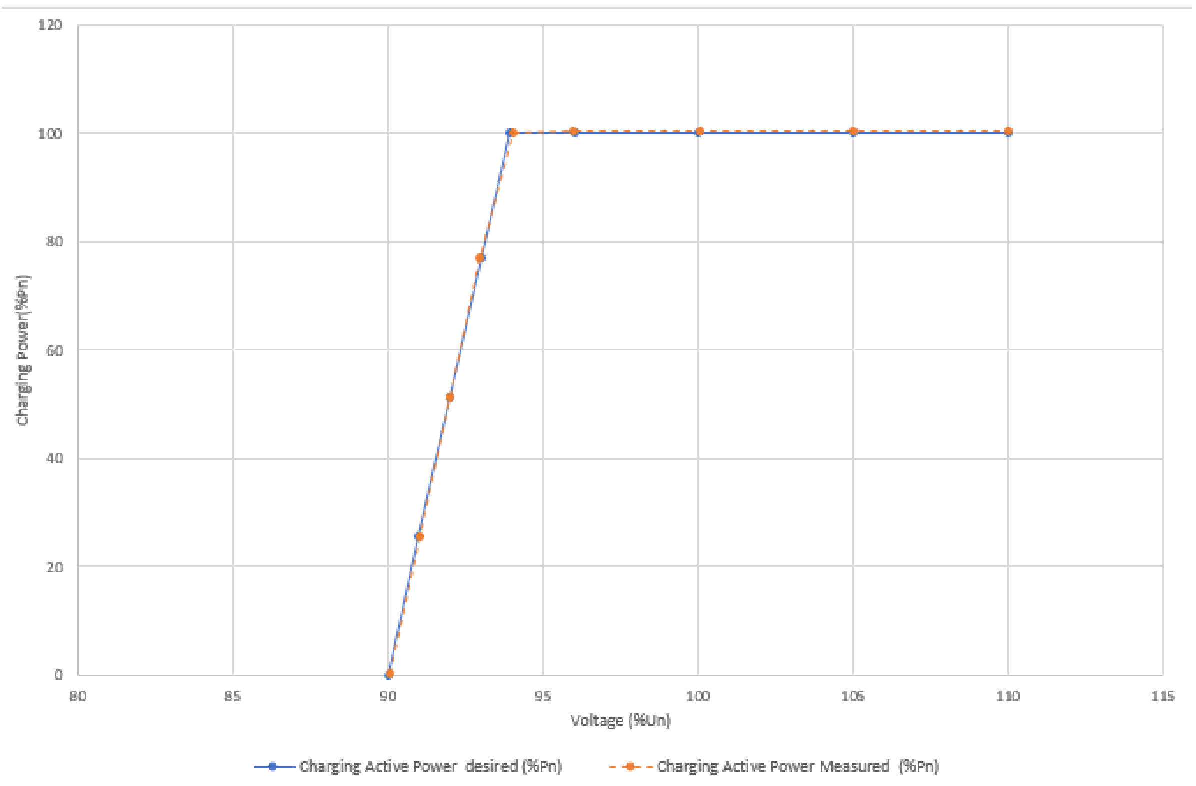
Reference	Test 1 Set points		Test 2 Set points	
	Volt. (%Un)	Power (%Pn)	Volt. (%Un)	Power (%Pn)
V1	90.0%	0%	90.1%	0%
V2	93.9%	100%	100.0%	100%
V3	105.0%	100%	105.0%	100%
V4	110.0%	100%	110.0%	100%

4.14.2.1 Test 1

Voltage desired (%Un)	Voltage Measured (%Un)	Charging Active Power desired (%Pn)	Charging Active Power Measured (%Pn)	Charging Active Power Deviation (%Pn)
90.0	90.0	0.0	0.3	0.3
91.0	91.0	25.6	25.7	0.1
92.0	92.0	51.3	51.3	0.0
93.0	93.0	76.9	77.0	0.1
94.0	94.0	100.0	100.2	0.2
96.0	96.0	100.0	100.5	0.5
100.0	100.1	100.0	100.5	0.5
105.0	105.0	100.0	100.5	0.5
110.0	110.0	100.0	100.6	0.6

Volt – Watt (Test 1)

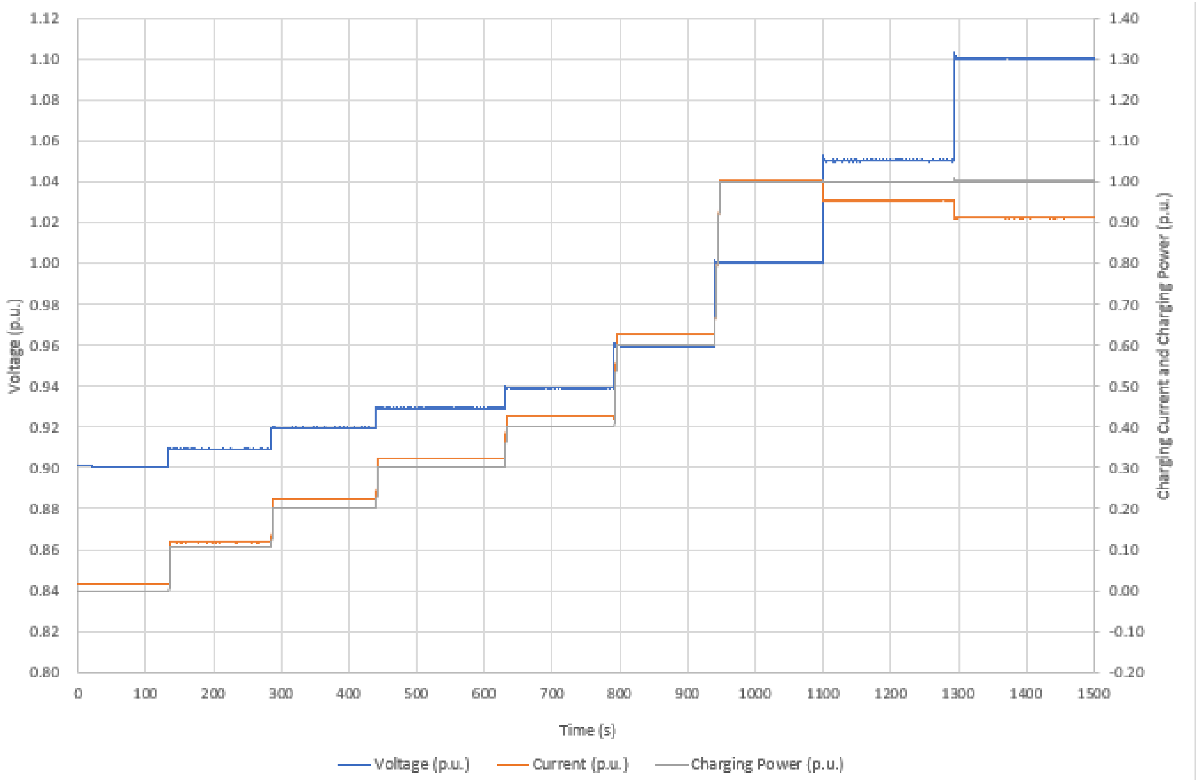


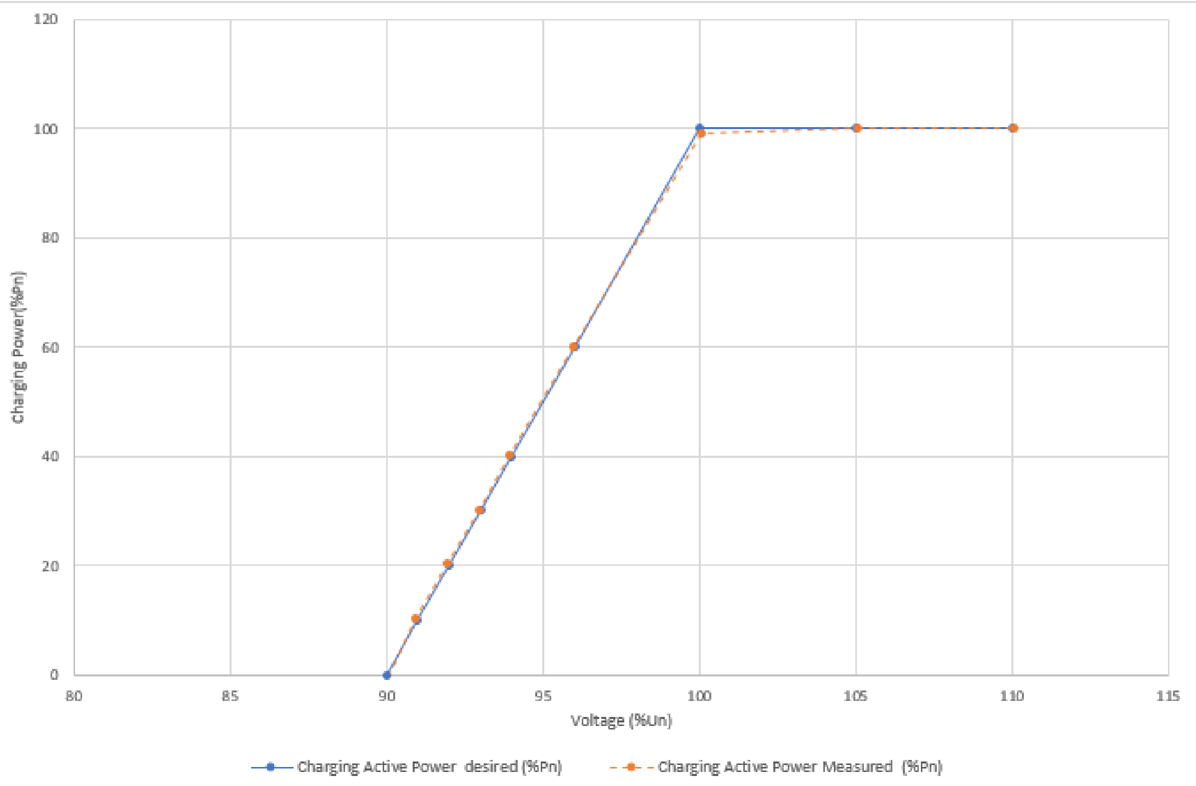


4.14.2.2 Test 2

Voltage desired (%Un)	Voltage Measured (%Un)	Charging Active Power desired (%Pn)	Charging Active Power Measured (%Pn)	Charging Active Power Deviation (%Pn)
90.0	90.1	0.0	-0.3	-0.3
91.0	90.9	10.0	10.4	0.4
92.0	92.0	20.0	20.3	0.3
93.0	92.9	30.0	30.1	0.1
94.0	93.9	40.0	40.2	0.2
96.0	96.0	60.0	59.9	-0.1
100.0	100.1	100.0	99.1	-0.9
105.0	105.1	100.0	100.2	0.2
110.0	110.0	100.0	100.2	0.2

Volt – Watt (Test 2)





4.15 SECURITY OF OPERATIONAL SETTINGS

According to the Clause 6.5 of the standard, it has been verified by inspection that changes to the internal setting may require the use of a tool and special instructions not provided to unauthorized personnel.

4.16 AUTOMATIC DISCONNECTION DEVICE

It has been verified that the automatic disconnection device meets the requirements stated in the Clause 7.2 of the standard.

This automatic disconnection device is in compliance with the following points:

- Is capable to withstand an impulse voltage that could occur at the point of installation and has the appropriate contact gap.
- It doesn't indicate falsely that contacts are open.
- It is installed and designed to prevent unintentional closure that can be caused by events such as impacts or vibration.
- It has devices that disconnects on all live conductors (active and neutral) of the inverter from the grid.
- It is ensured that in case of single fault, there is simple separation.
- It is ensured that in case of single fault, power is prevented to entering the grid.
- It is capable of interrupting the rated current of the equipment.
- The settings of the automatic disconnection don't exceed the capability of the inverter.
- There are not used solid-state semiconductors for isolation purposes.

4.17 ACTIVE ANTI-ISLANDING PROTECTION

Test performed according to IEC 62116. The method used to provide active anti-islanding is frequency instability.

It has been done three different tests,

- Test A (Active Power >90% Pn and Input Voltage > 75% Vdc)
- Test B (Active Power 50-66% Pn and Input Voltage 50±10% Vdc)
- Test C (Active Power 25-33% Pn and Input Voltage < 20% Vdc)

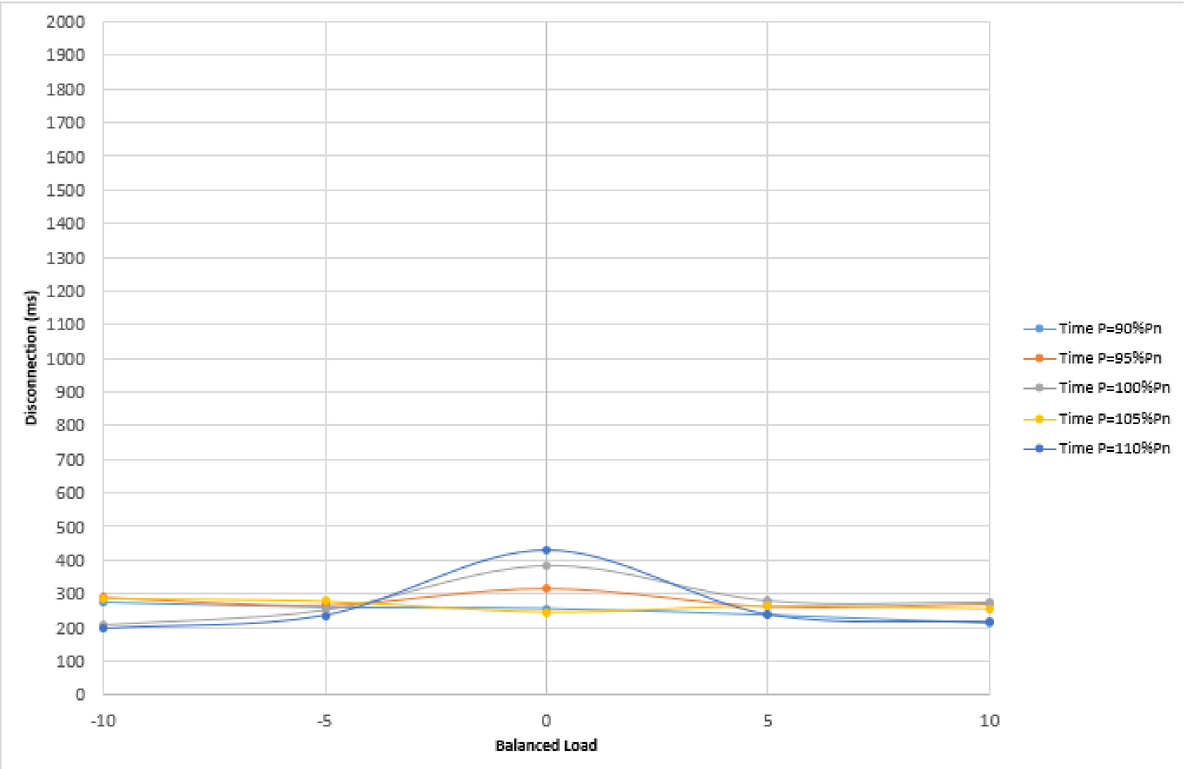
The maximum trip time is 2 s.

Note: In the tables below, M(%) and N(%) are respectively referred to active and reactive power impedance variation as percentage.

4.17.1 Test A

Balanced Load		
M (%)	**N (%)**	**Disconnection (ms) (limit at t=2s)**
-10	-10	274
-10	-5	260
-10	0	256
-10	+5	238
-10	+10	214
-5	-10	290
-5	-5	268
-5	0	316
-5	+5	264
-5	+10	272
0	-10	208
0	-5	252
0	0	386
0	+5	280
0	+10	276
+5	-10	286
+5	-5	278
+5	0	244
+5	+5	264
+5	+10	254
+10	-10	196
+10	-5	236
+10	0	432
+10	+5	238
+10	+10	216

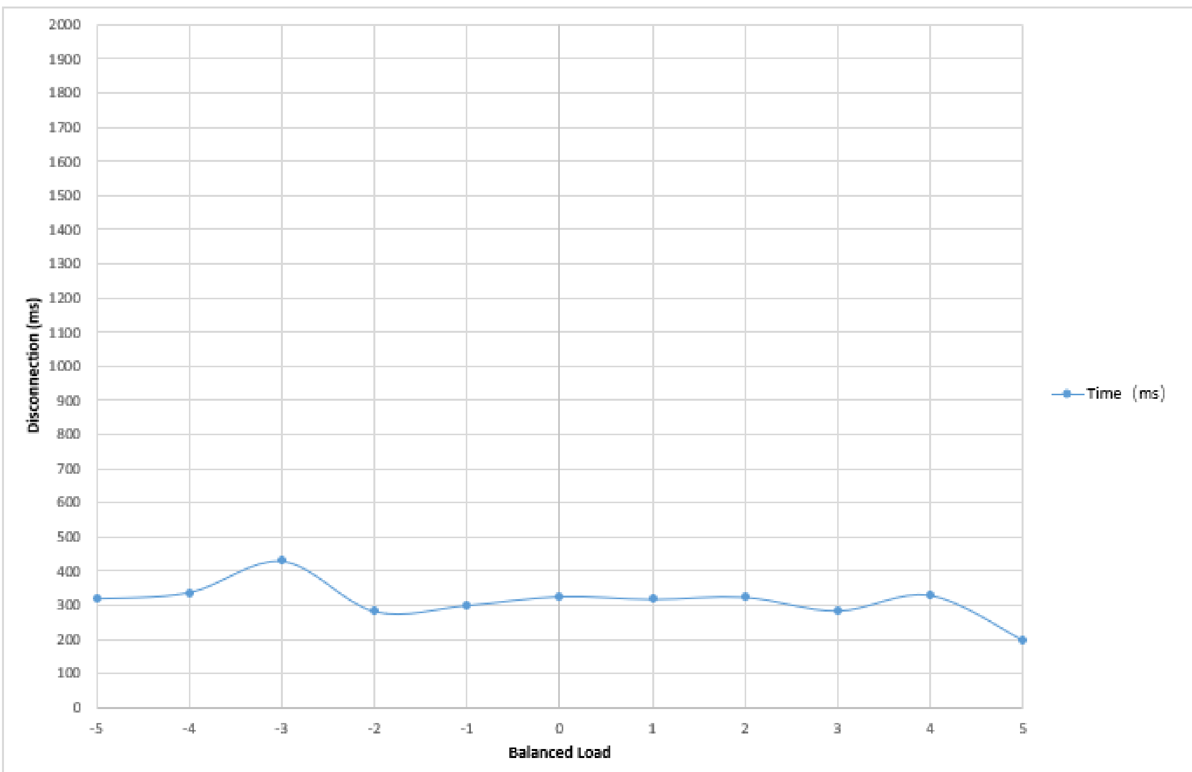
Test A


2000
1900
1800
1700
1600
1500
1400
1300
1200
1100
1000
900
800
700
600
500
400
300
200
100
0
Disconnection (ms)
-10
-5
0
5
10
Balanced Load
Time P=90%Pn
Time P=95%Pn
Time P=100%Pn
Time P=105%Pn
Time P=110%Pn

4.17.2 Test B

Balanced Load		
M (%)	N (%)	Disconnection (ms) (limit at t=2s)
0	-5	320
0	-4	338
0	-3	430
0	-2	282
0	-1	300
0	0	326
0	1	318
0	2	324
0	3	284
0	4	330
0	5	198

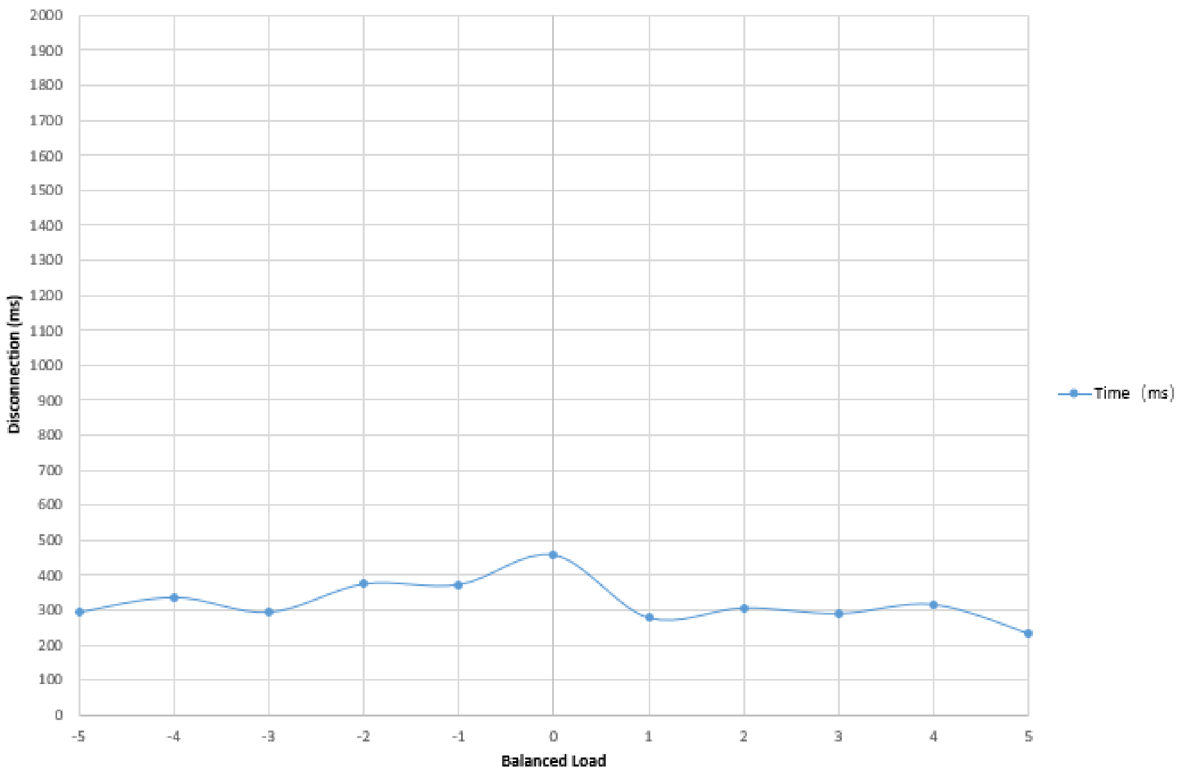
Test B



4.17.3 Test C

Balanced Load		
M (%)	N (%)	Disconnection (ms) (limit at t=2s)
0	-5	294
0	-4	336
0	-3	294
0	-2	374
0	-1	372
0	0	456
0	1	278
0	2	306
0	3	290
0	4	316
0	5	234

Test C



4.18 VOLTAGE AND FREQUENCY LIMITS (PASSIVE ANTI-ISLANDING PROTECTION)

Voltage and frequency limits (Passive Anti-islanding Protection) have been verified according to the Clause 7.4 of the standard.

The inverter should remain in continuous and uninterrupted operation for voltage and frequency variations with duration shorter than the trip delay time specified in the next table:

Protective function	Protective function limit	Trip delay time	Maximum disconnection time
Undervoltage (V<)	180 V	1 s	2 s
Overvoltage 1 (V>)	260 V	1 s	2 s
Overvoltage 2 (V>>)	265 V	—	0.2 s
Under-frequency (F<)	47 Hz (Australia) 45 Hz (New Zealand)	1 s	2 s
Over-frequency (F>)	52 Hz	—	0.2 s

Voltage limits stated by the standard have been expressed as a percentage of 230V and applied to the rated values of the family of inverters contemplated in this report.

Each test should be repeated 3 times.

Following indications shall be taken into account to for test results offered in this point.

For trip tests evaluation it is considered the time from when the voltage or frequency, as proceed, is stabilized at the setting value to the instant when the inverter is effectively disconnected and with no current.

For frequency trip tests evaluation, in order to have a bigger accuracy it has been evaluated and represented the first period of the sine wave where the frequency surpasses the frequency limit and from that first period has been evaluated the tripping time.

For these cases, a second graph representing the “trip value” is offered. In them cursors are allocated among the beginning and the end of a period of the voltage sine wave, measuring the time that lasts the whole period and allowing calculating the frequency of the period.

4.18.1 Voltage trip tests

To asses that the protective function of the inverter against abnormal voltage is effective two different kinds of tests have been done:

- Trip value tests to evaluate if the inverter can trip with accuracy in accordance with a settling value of voltage.
- Trip time tests to evaluate if the inverter can trip into the limits of time stated by the standard in case of detecting voltage levels out of the limits stated.

The standard states that the tolerance limit for voltage trip values is ± 2 V, which is a 0.8% Un over 230 V, the reference voltage considered by the standard. So 0.8% Un is the allowed tolerance to be considered for voltage trip value tests.

4.18.1.1 Voltage trip value tests

The tests have been made as the following procedure:

- For undervoltage protection (U<): Starting from a voltage level 1% Un above the trip value of the protection function to be tested, the voltage is decreased 1V in steps of at least 5 seconds.
- For overvoltage protection (U>): Starting from a voltage level 1% Un below the trip value of the protection function to be tested, the voltage is increased 1V in steps of at least 5 seconds.
- For overvoltage protection (U>>): Starting from a voltage level 1% Un below the trip value of the protection function to be tested, the voltage is increased 1V in steps of at least 5 seconds. Disable overvoltage protection (U>) function during the test.

Test results are offered in the following table:

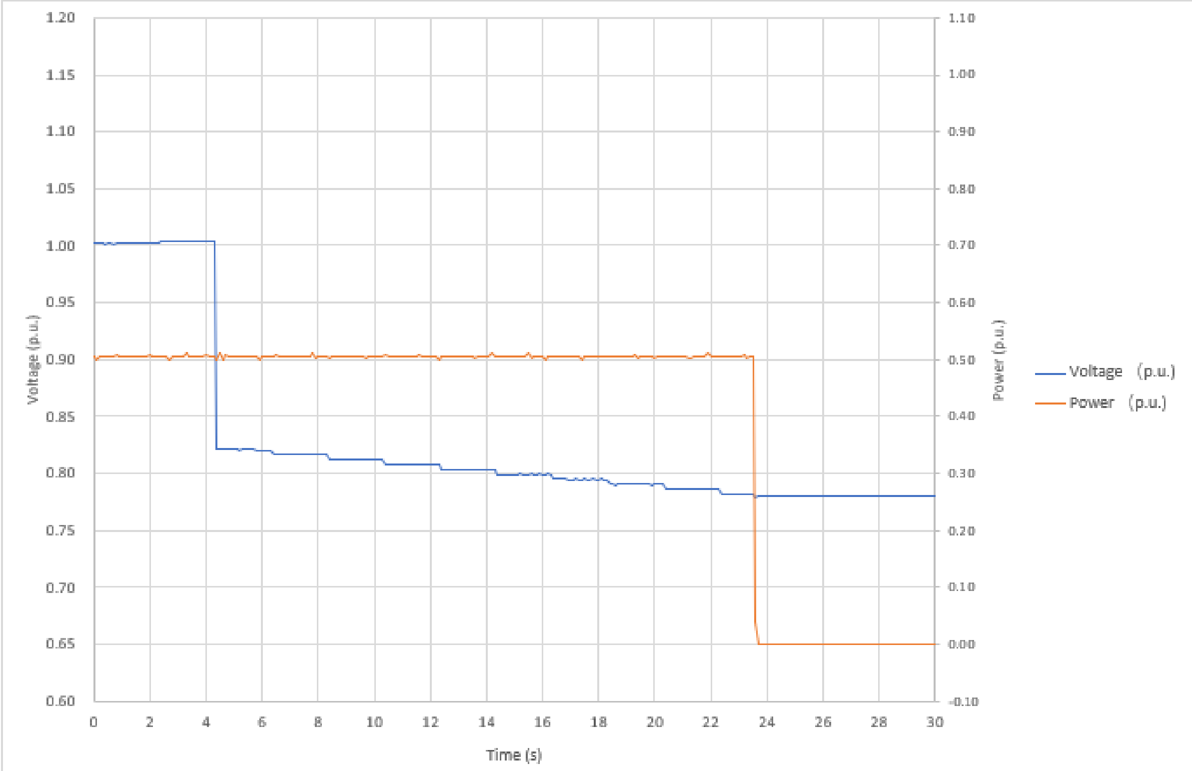
Protective Function Tested	No Trip Test			Trip Test		
	Start Voltage value (%Un)	Time measured per step (s) (**)	Trip	Voltage Trip settling value (%Un)	Trip	Voltage trip value measured (%Un)
U < (Rep 1)	79.5%	>2.00	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	78.0%
U < (Rep 2)	79.5%	>2.00	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	78.0%
U < (Rep 3)	79.5%	>2.00	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	78.0%
U > (Rep 1)	112.0%	>2.00	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	112.8%
U > (Rep 2)	112.0%	>2.00	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	112.8%
U > (Rep 3)	112.0%	>2.00	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	112.8%
U > > (Rep 1) (*)	114.0%	>2.00	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	115.0%
U > > (Rep 2) (*)	114.0%	>2.00	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	115.0%
U > > (Rep 3) (*)	114.0%	>2.00	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	115.0%

Note: Maximum deviation allowed in voltage trip value is ± 0.8% Un.

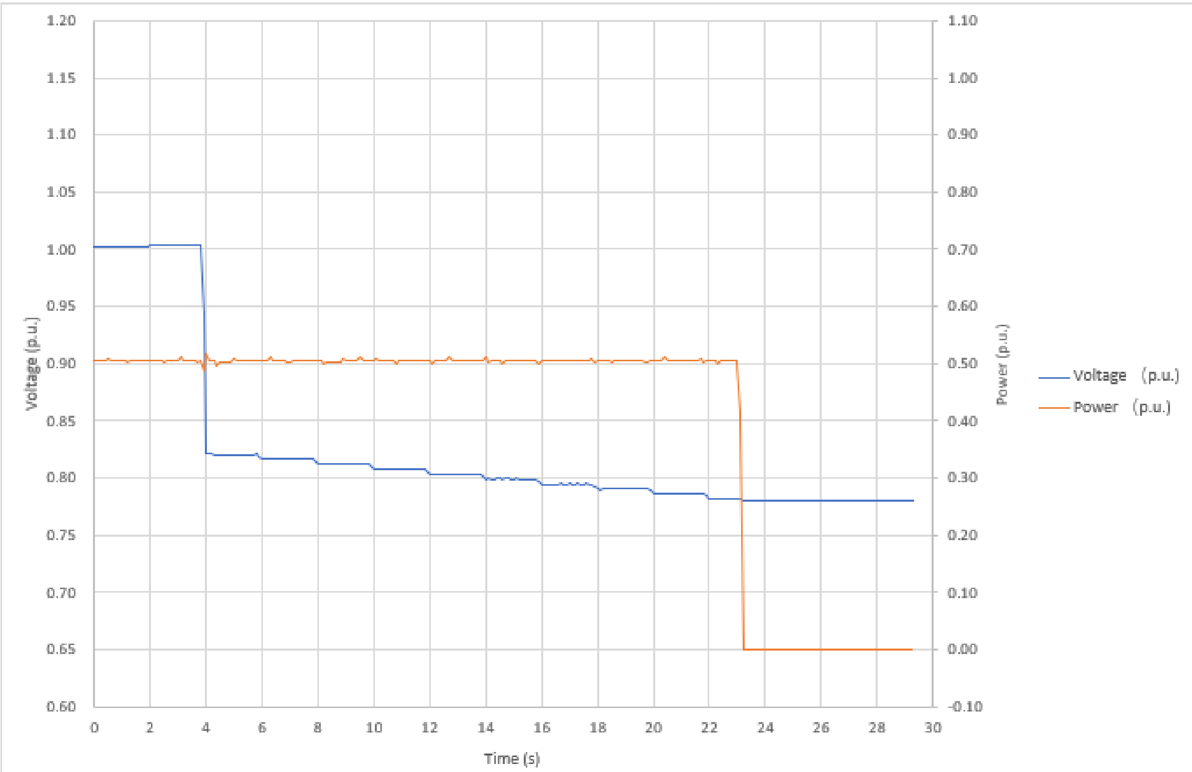
(*) Disable overvoltage protection (U>) function during the test.
(**) This time is enough to see that the inverter doesn’t trip in this voltage level.

Test results are graphically shown in following pages.

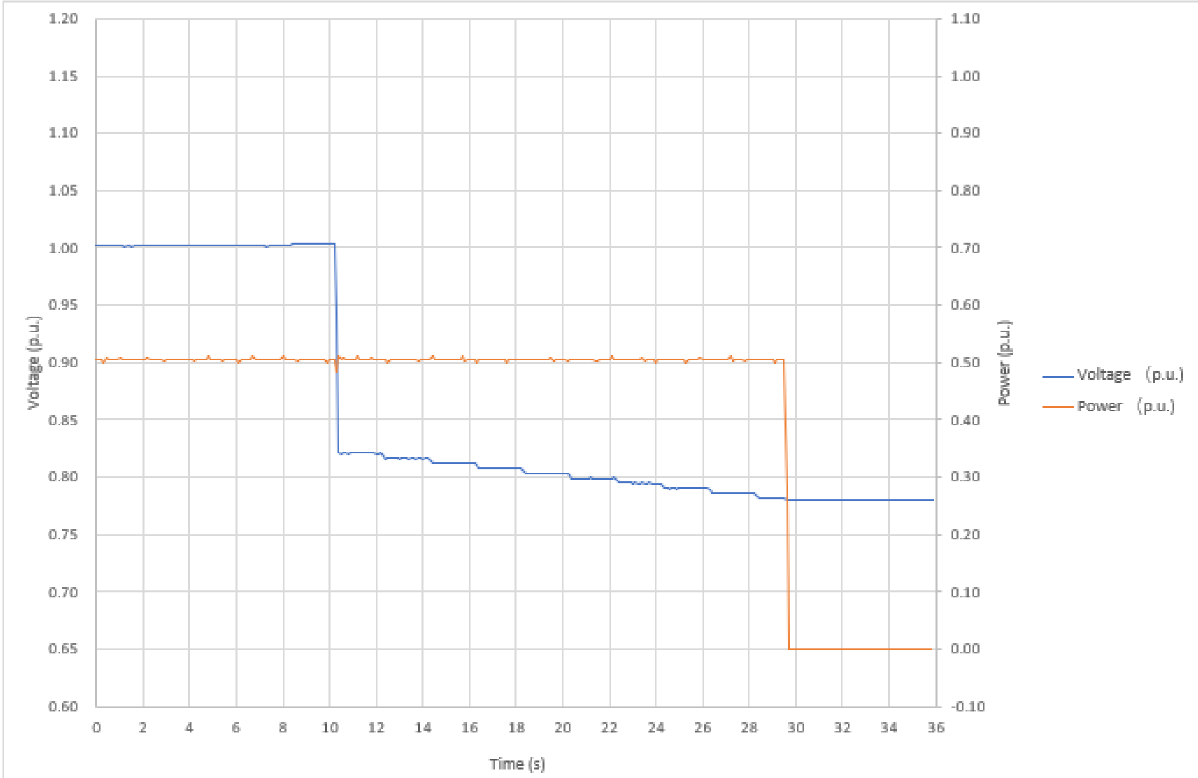
Undervoltage (U <) Rep 1



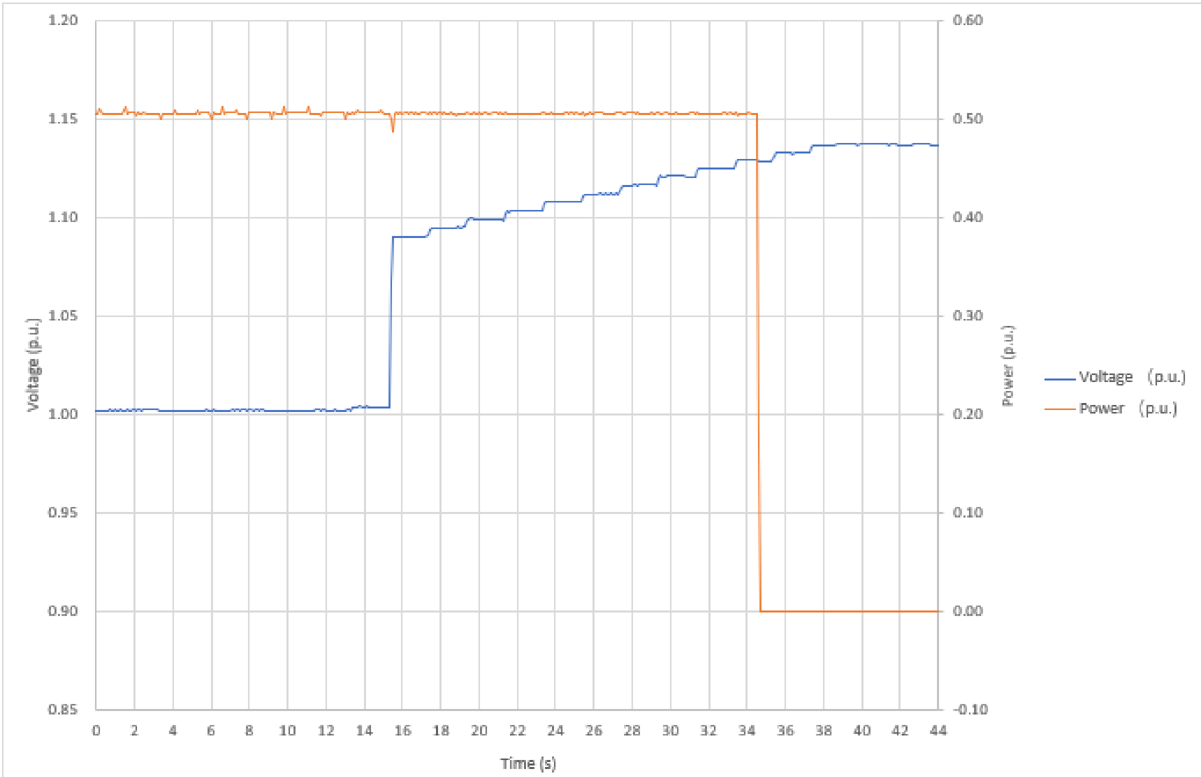
Undervoltage (U <) Rep 2



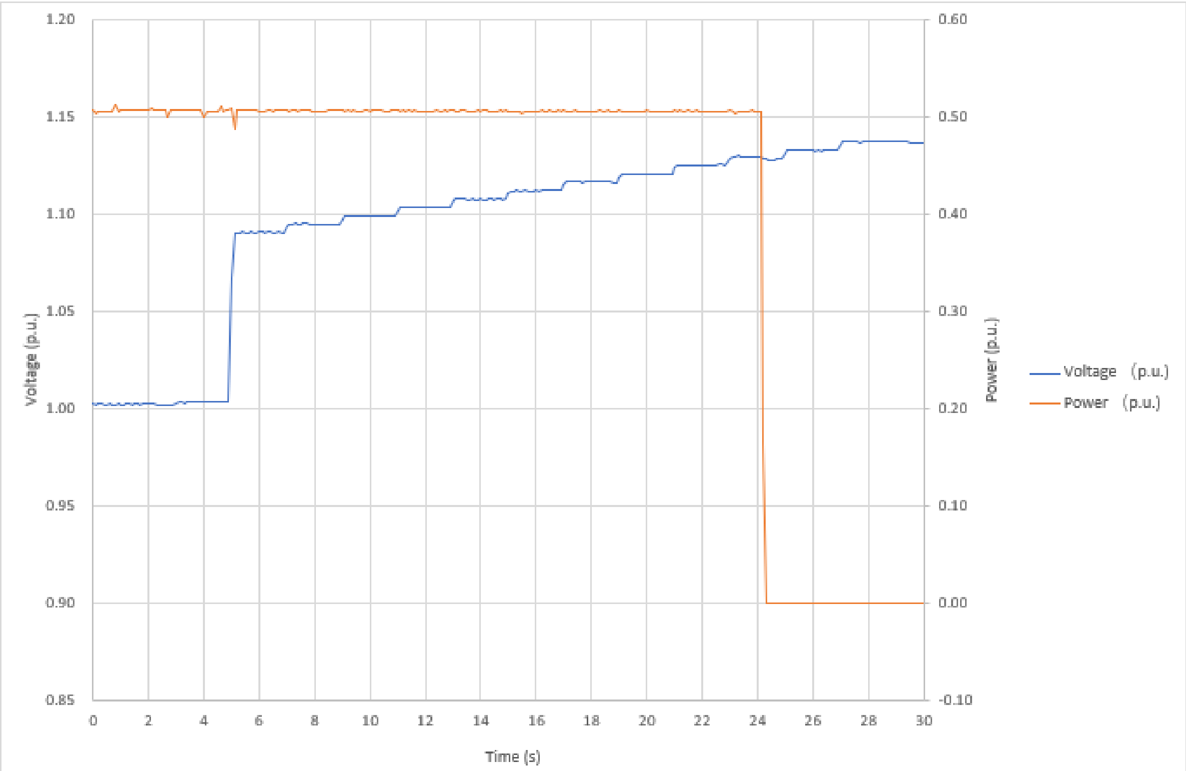
Undervoltage (U <) Rep 3



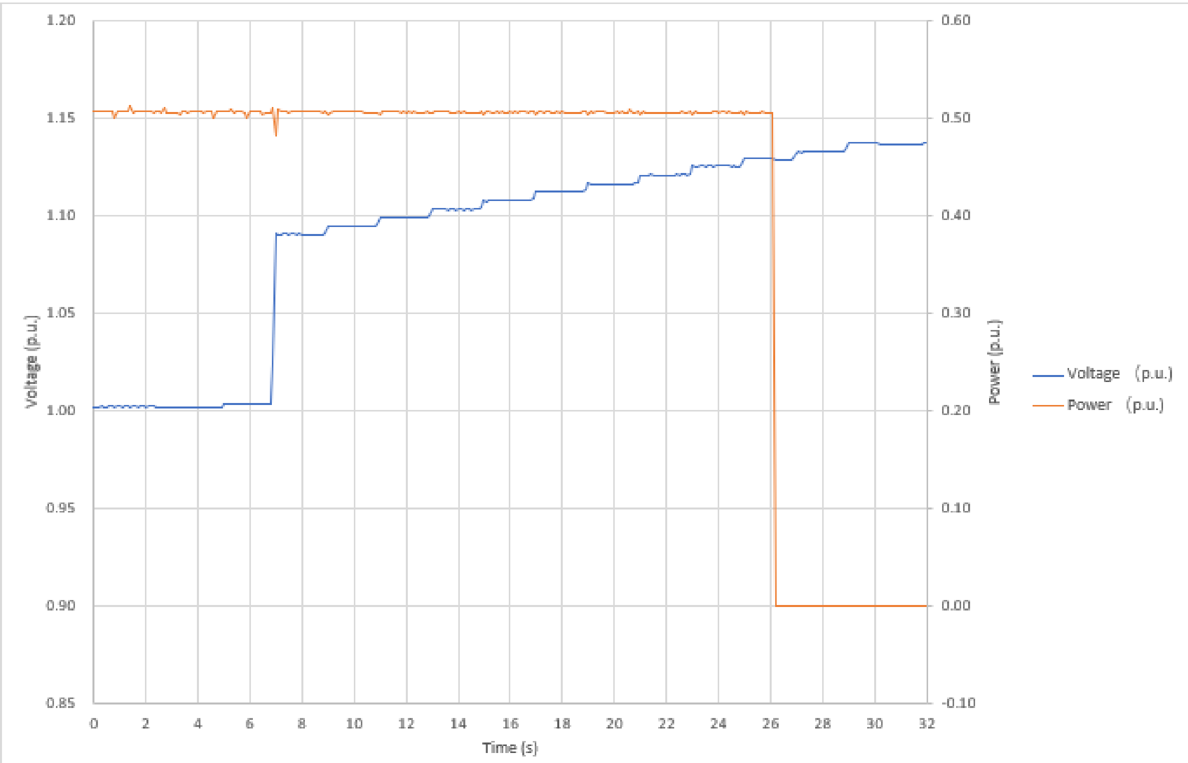
Overvoltage (U >) Rep 1



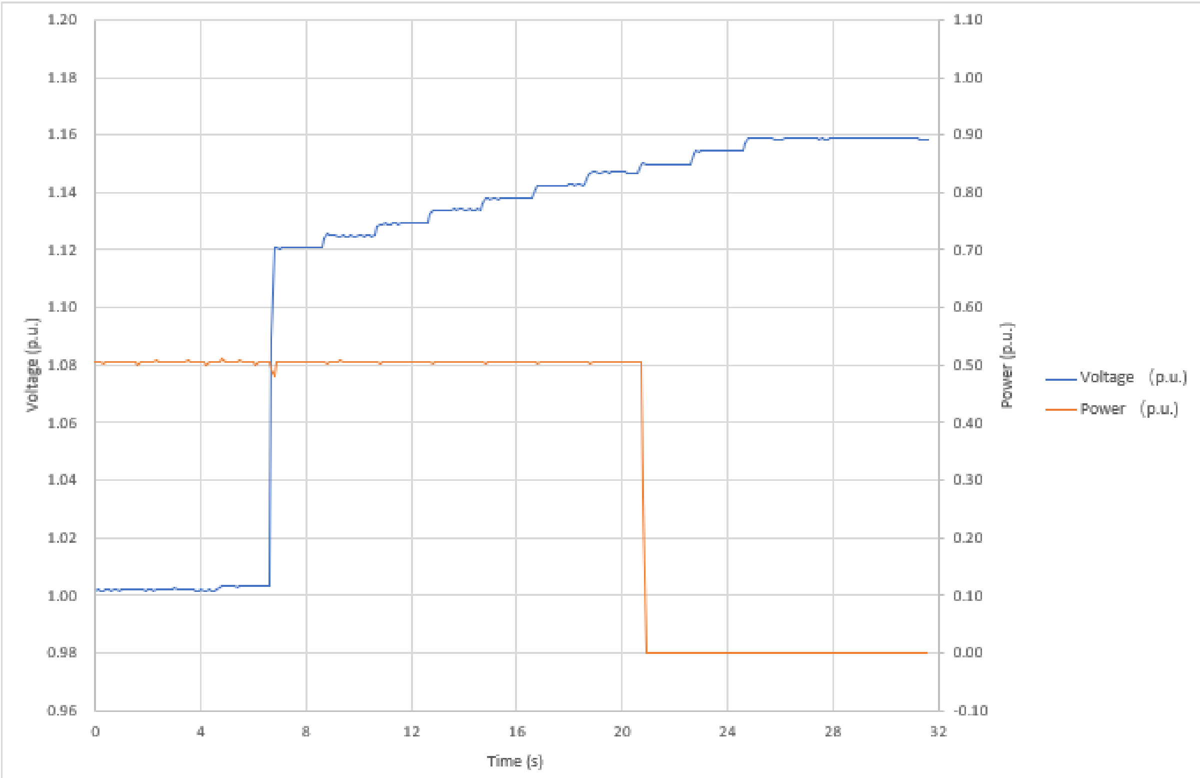
Overvoltage (U >) Rep 2



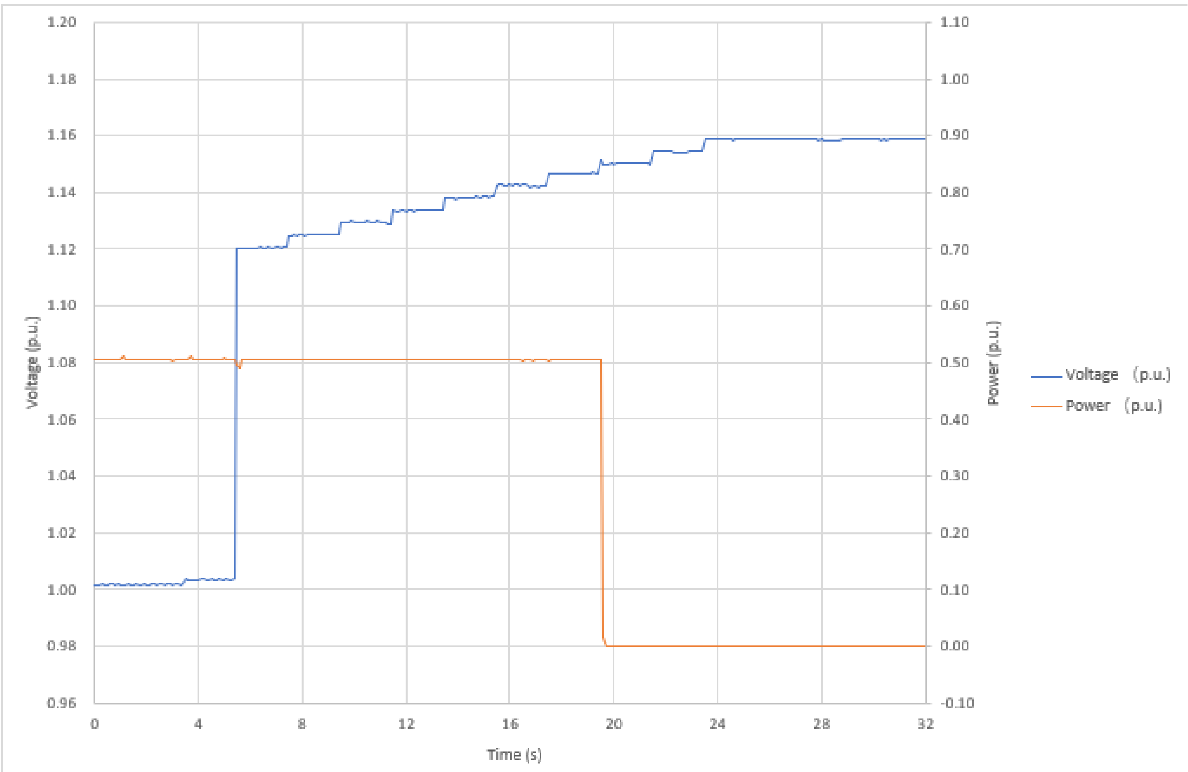
Overvoltage (U >) Rep 3



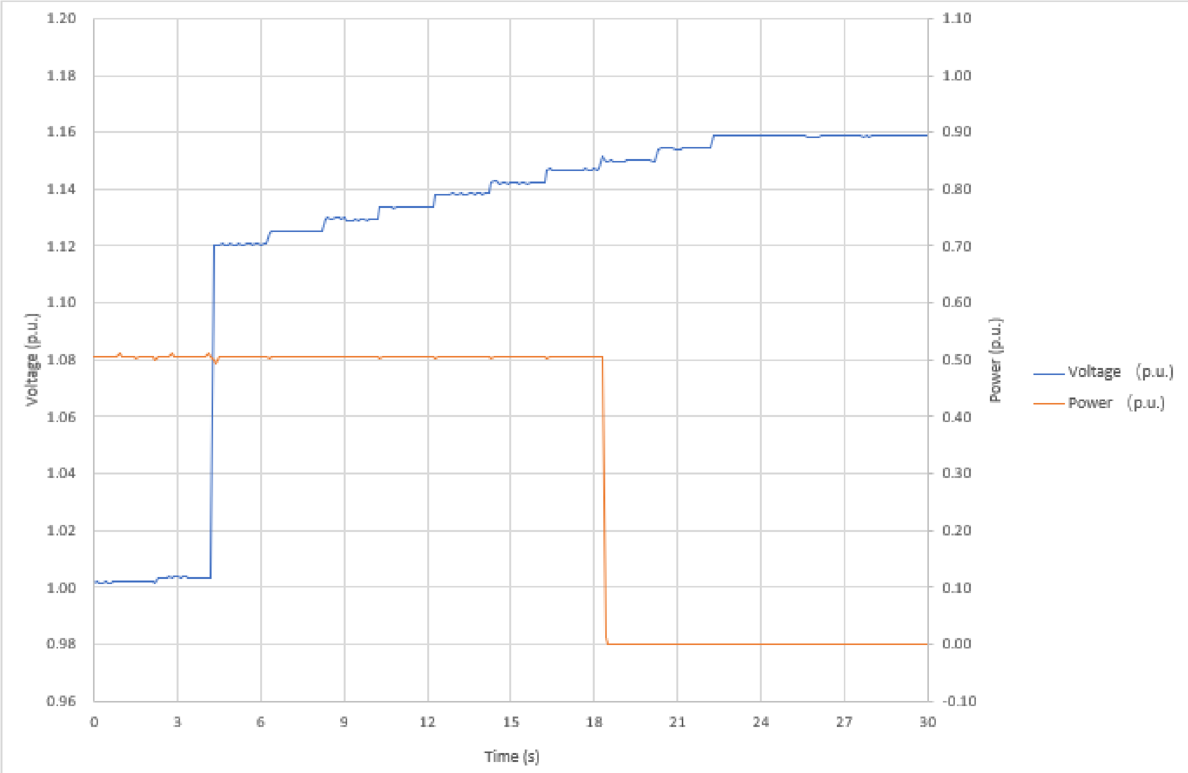
Overvoltage (U >>) Rep 1



Overvoltage (U >>) Rep 2



Overvoltage (U >>) Rep 3



4.18.1.2 Voltage trip time tests

The tests have been made as the following procedure:

- For undervoltage protection (U<): Maintaining the voltage with a value 78.5%Un during at least 1.5 seconds and then change the voltage to 78.2%Un with a step. Trip time shall take place in less than 2 seconds and more than 1s.

- For overvoltage protection (U>): Maintaining the voltage with a value 112.5%Un during at least 1.5 seconds and then change the voltage to 113.0%Un with a step. Trip time shall take place in less than 2 seconds and more than 1s.

- For overvoltage protection (U>>): Maintaining the voltage with a value 114.5%Un during at least 0.5 seconds and then change the voltage to 115.0%Un with a step. Trip time shall take place in less than 0.2 seconds.

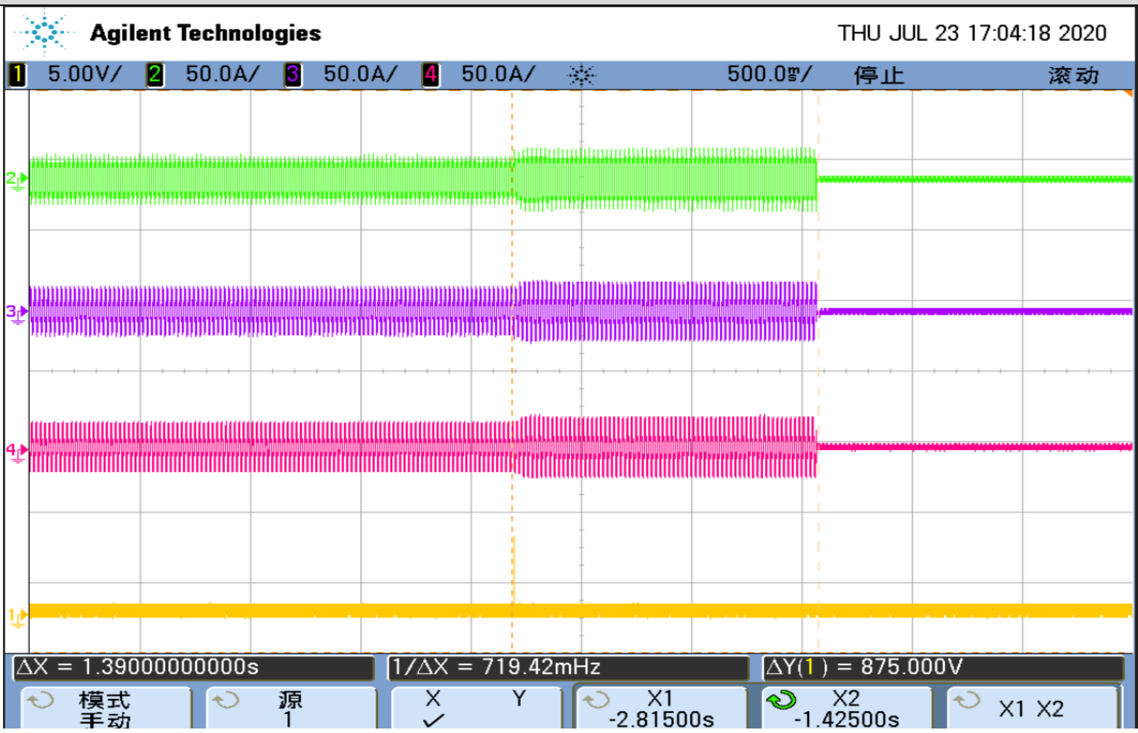
Test results are offered in the following table:

Protective Function Tested	No Trip Test			Trip Test		
	Voltage value (%Un)	Time measured (s) (*)	Trip	Voltage settling value (%Un)	Trip	Trip time measured (ms)
U < (Rep 1)	78.5%	>1.5	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	1390
U < (Rep 2)	78.5%	>1.5	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	1410
U < (Rep 3)	78.5%	>1.5	☒ NO ☐ YES	78.3%	☐ NO ☒ YES	1270
U > (Rep 1)	112.5%	>1.5	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	1225
U > (Rep 2)	112.5%	>1.5	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	1250
U > (Rep 3)	112.5%	>1.5	☒ NO ☐ YES	113.0%	☐ NO ☒ YES	1235
U > > (Rep 1)	114.5%	> 0.5	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	140
U > > (Rep 2)	114.5%	> 0.5	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	123
U > > (Rep 3)	114.5%	> 0.5	☒ NO ☐ YES	115.0%	☐ NO ☒ YES	122

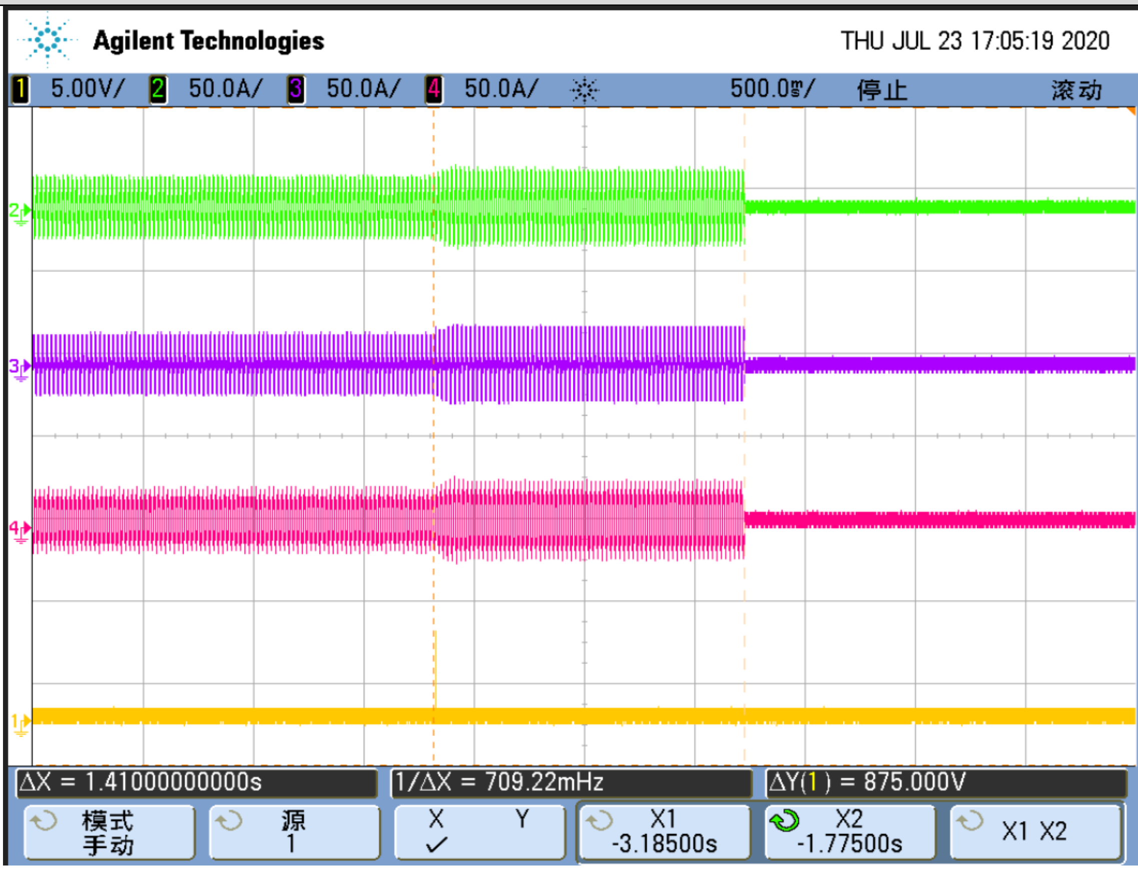
Test results are graphically shown in the graph below and in the following page.

(*) This time is enough to see that the inverter doesn’t trip in this voltage level.

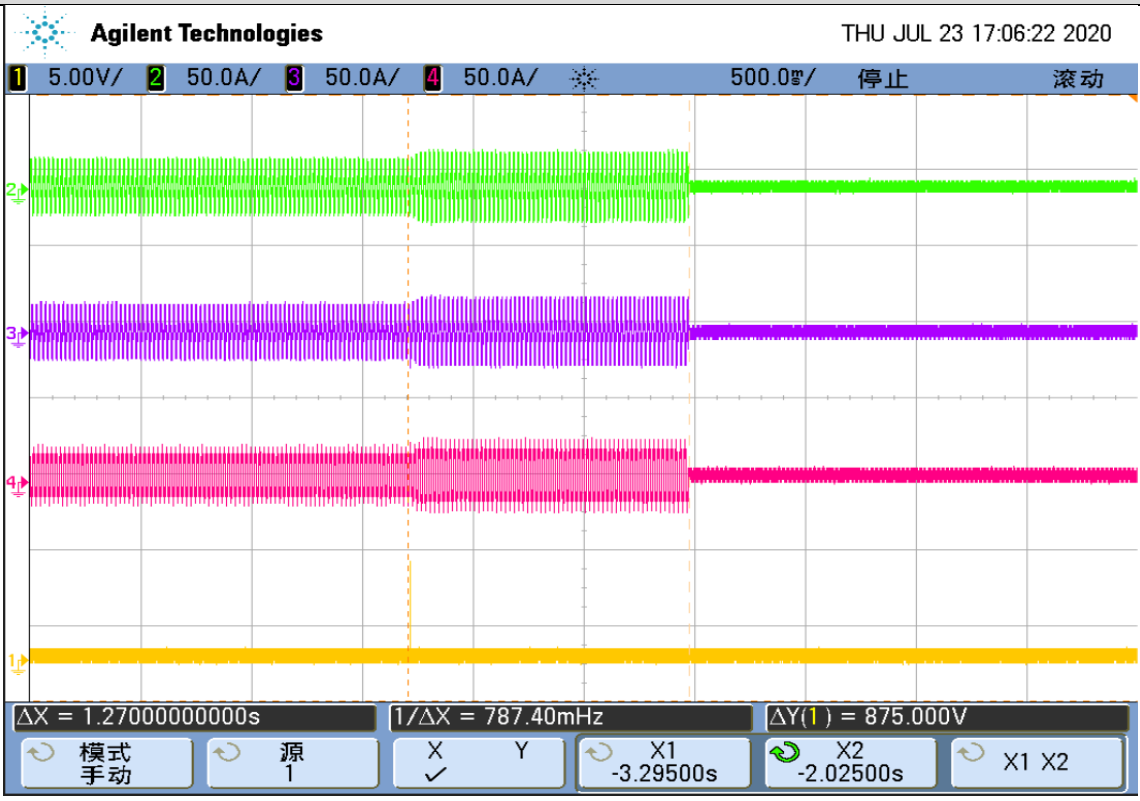
Undervoltage (U <) Rep 1



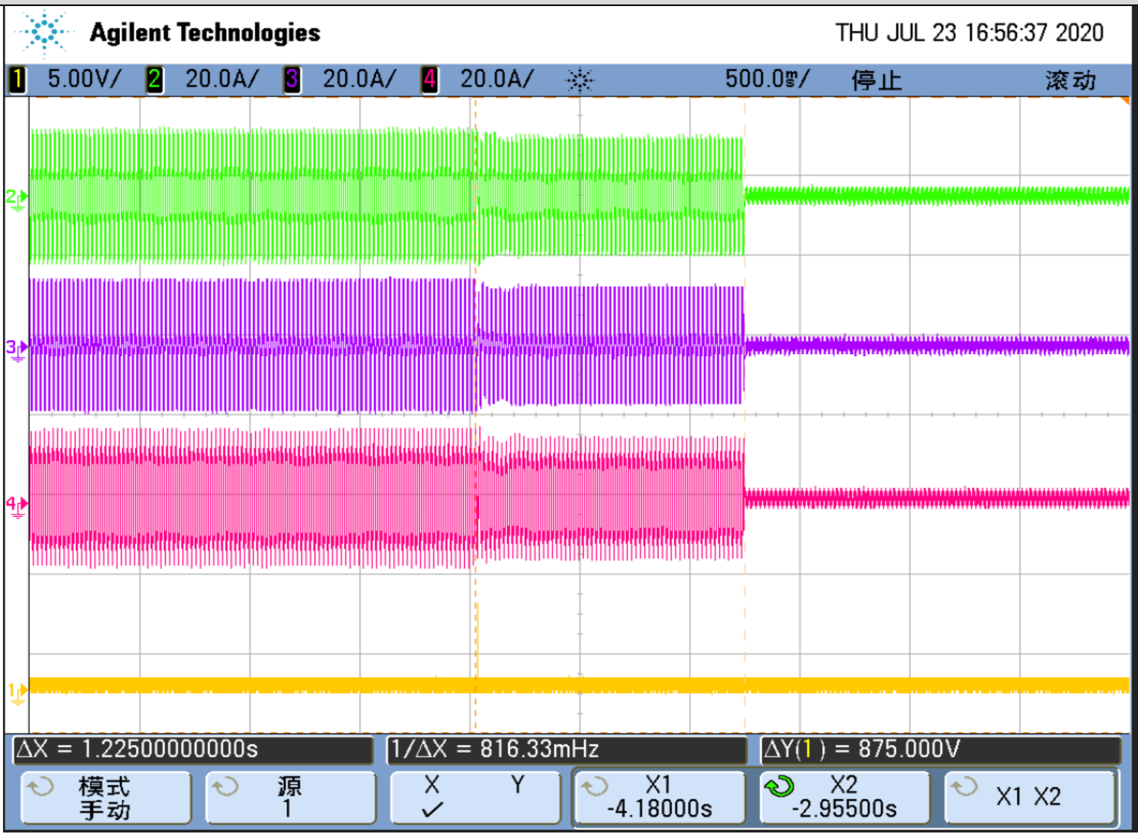
Undervoltage (U <) Rep 2



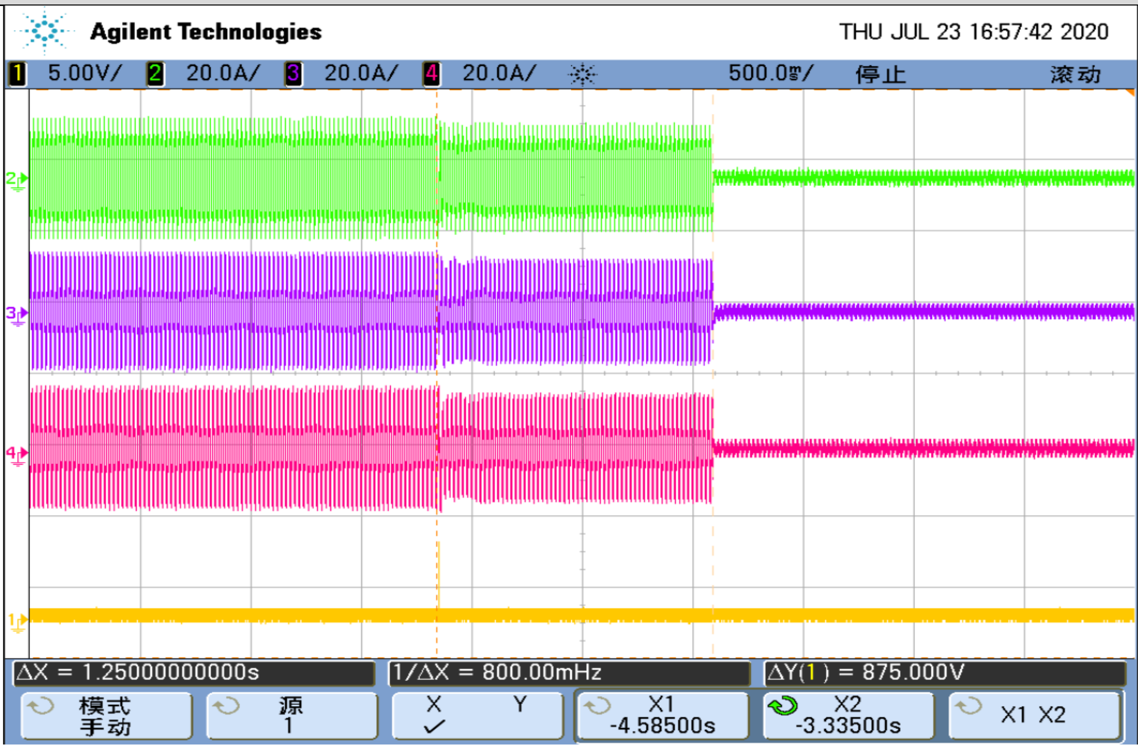
Undervoltage (U<) Rep 3



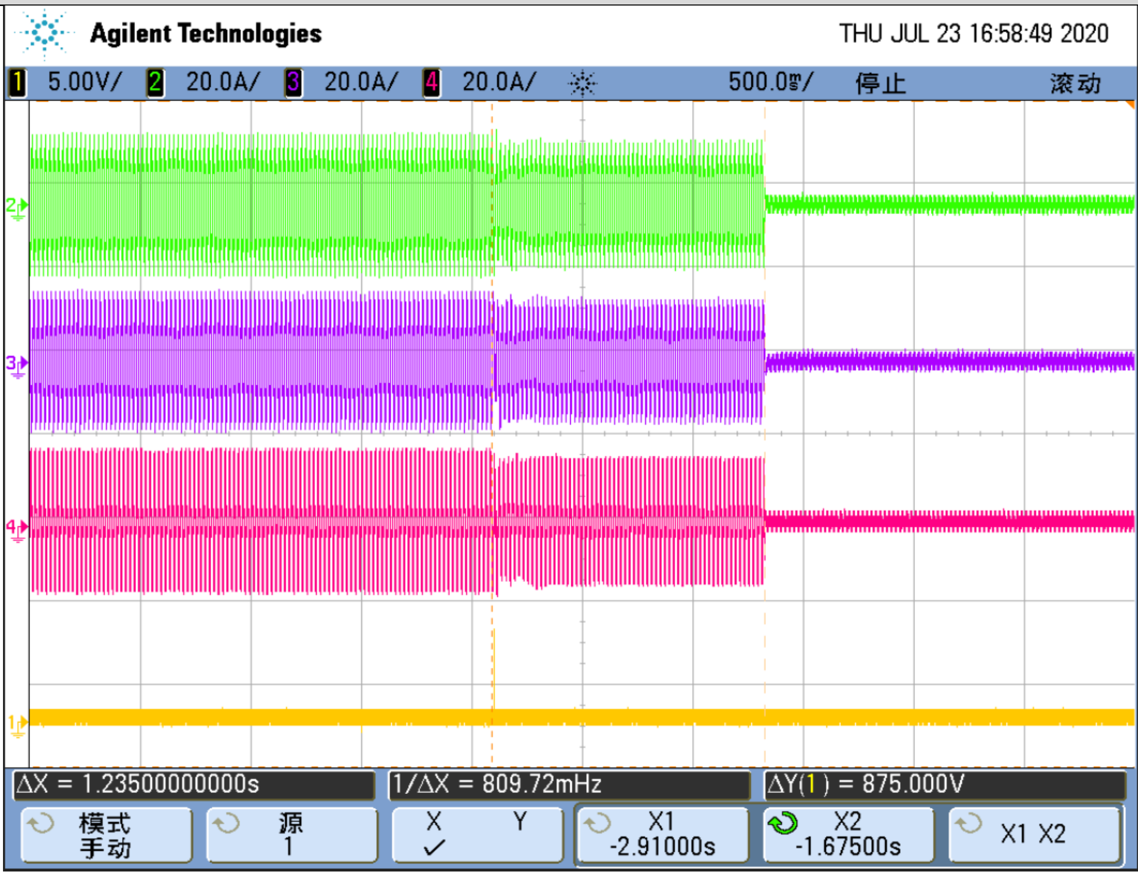
Overvoltage (U>) Rep 1



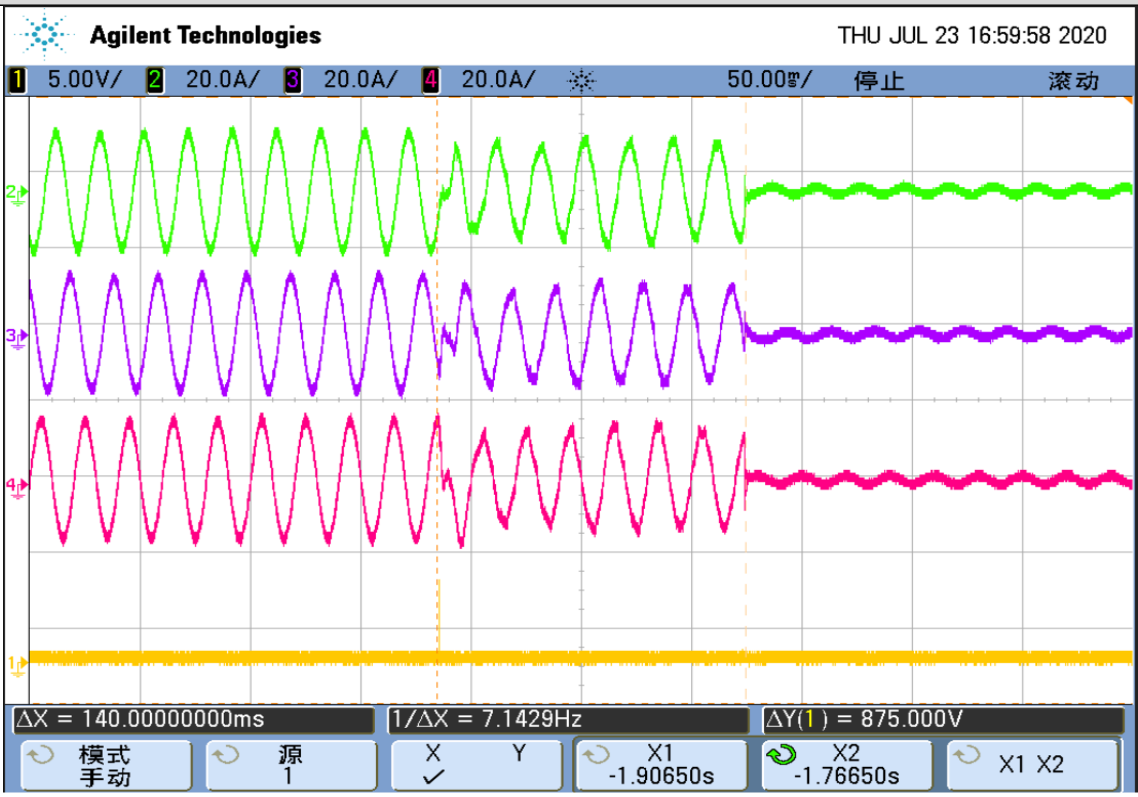
Overvoltage (U>) Rep 2



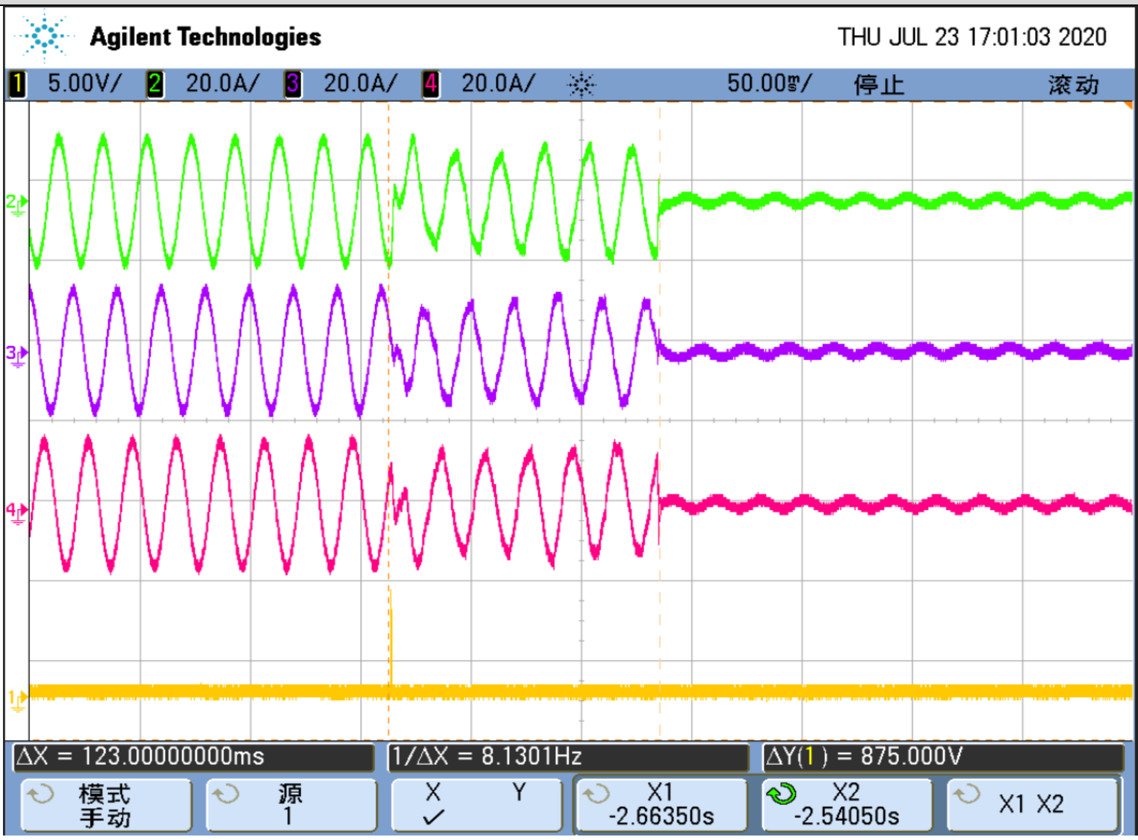
Overvoltage (U>) Rep 3



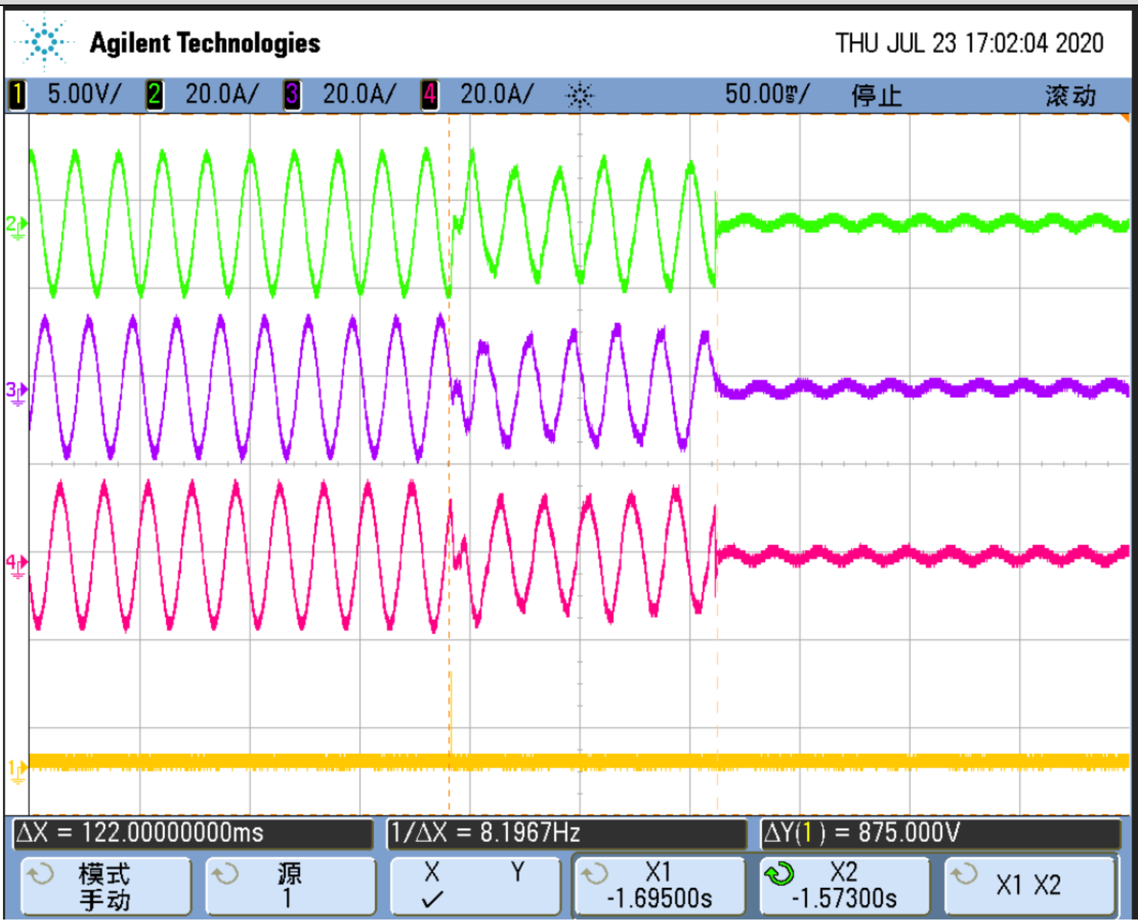
Overvoltage (U>>) Rep 1



Overvoltage (U>>) Rep 2



Overvoltage (U>>) Rep 3



4.18.2 Frequency trip tests

To asses that the protective function of the inverter against abnormal frequency is effective two different kinds of tests have been done:

- Trip value tests, to evaluate if the inverter can trip with accuracy in accordance with a settling value of frequency.
- Trip time tests, to evaluate if the inverter can trip into the limits of time stated by the standard in case of detecting frequency levels out of the limits stated by the standard.

4.18.2.1 Frequency trip value tests

The tests have been made as the following procedure:

- For underfrequency protection: Starting from a frequency level 0.2 Hz above the trip value of the protection function to be tested, the frequency is decreased 0.05 Hz in steps of at least 150% of the trip time delay stated in the protection function to be tested.

- For overfrequency protection: Starting from a frequency level 0.2 Hz below the trip value of the protection function to be tested, the frequency is increased 0.05 Hz in steps of at least 150% of the trip time delay stated in the protection function to be tested.

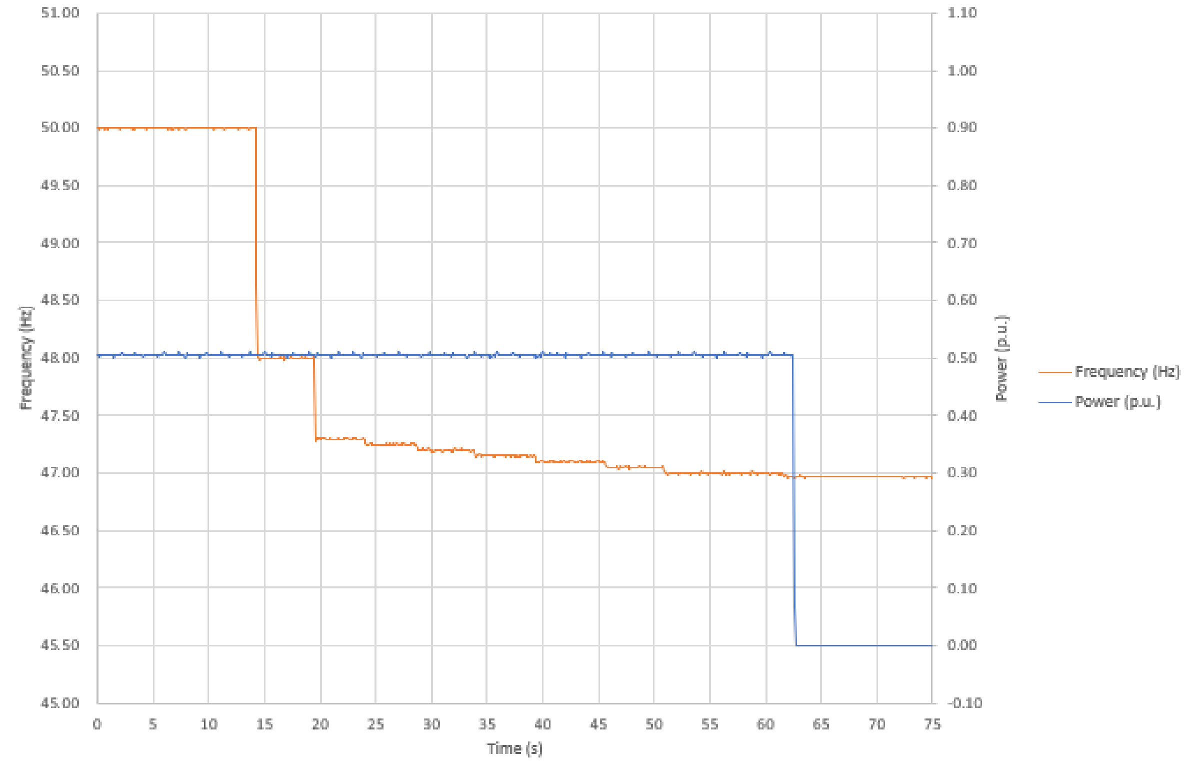
Test results are offered in the following tables:

Protective Function Tested	No Trip Test			Trip Test		
	Frequency value (Hz)	Time measured (s)	Trip	Frequency settling value (Hz)	Trip	Frequency trip value measured (Hz)
F< (Rep1) Australia	47.20	> 5.0	☒ NO ☐ YES	47.00	☐ NO ☒ YES	46.97
F< (Rep2) Australia	47.20	> 5.0	☒ NO ☐ YES	47.00	☐ NO ☒ YES	46.97
F< (Rep3) Australia	47.20	> 5.0	☒ NO ☐ YES	47.00	☐ NO ☒ YES	46.97
F< (Rep1) New Zealand	45.20	> 5.0	☒ NO ☐ YES	45.00	☐ NO ☒ YES	44.97
F< (Rep2) New Zealand	45.20	> 5.0	☒ NO ☐ YES	45.00	☐ NO ☒ YES	44.97
F< (Rep3) New Zealand	45.20	> 5.0	☒ NO ☐ YES	45.00	☐ NO ☒ YES	44.97
F> (Rep1)	51.80	> 5.0	☒ NO ☐ YES	52.00	☐ NO ☒ YES	52.00
F> (Rep2)	51.80	> 5.0	☒ NO ☐ YES	52.00	☐ NO ☒ YES	52.00
F> (Rep3)	51.80	> 5.0	☒ NO ☐ YES	52.00	☐ NO ☒ YES	52.00

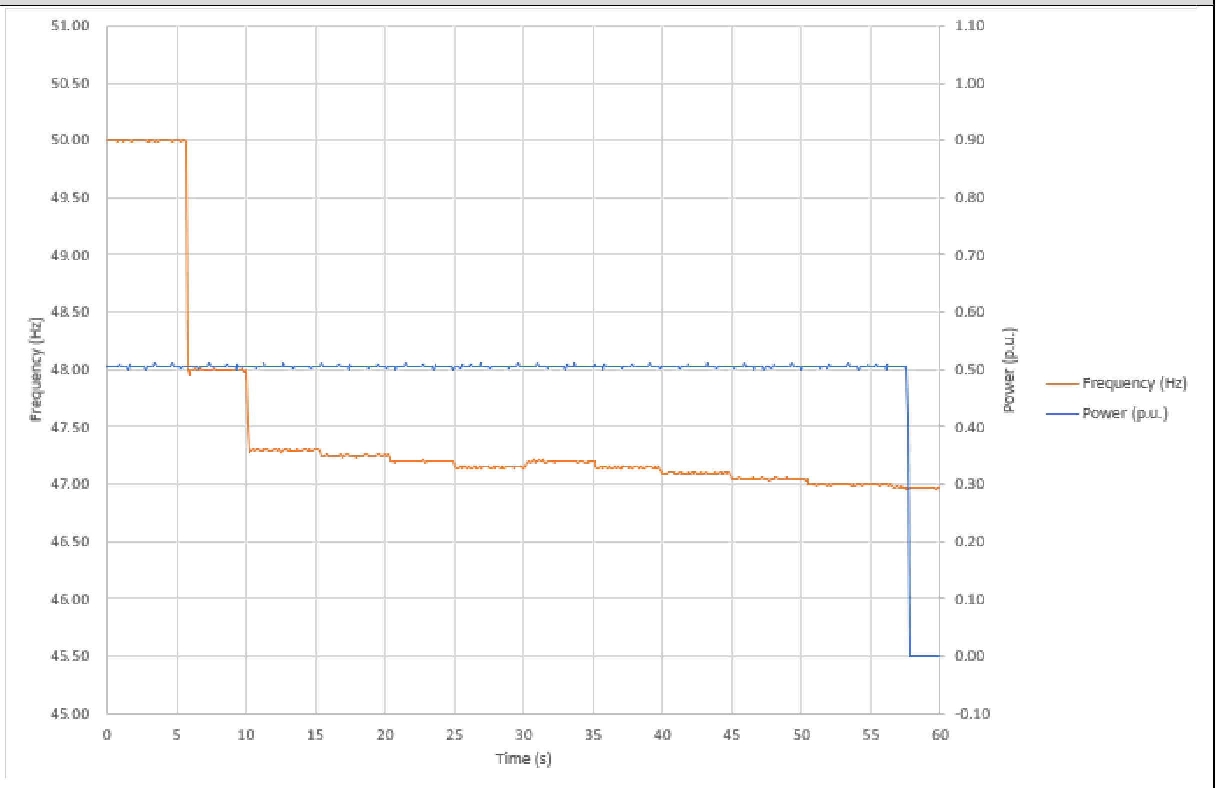
Maximum frequency deviation allowed is ±0.10 Hz.

Test results are graphically shown in following pages.

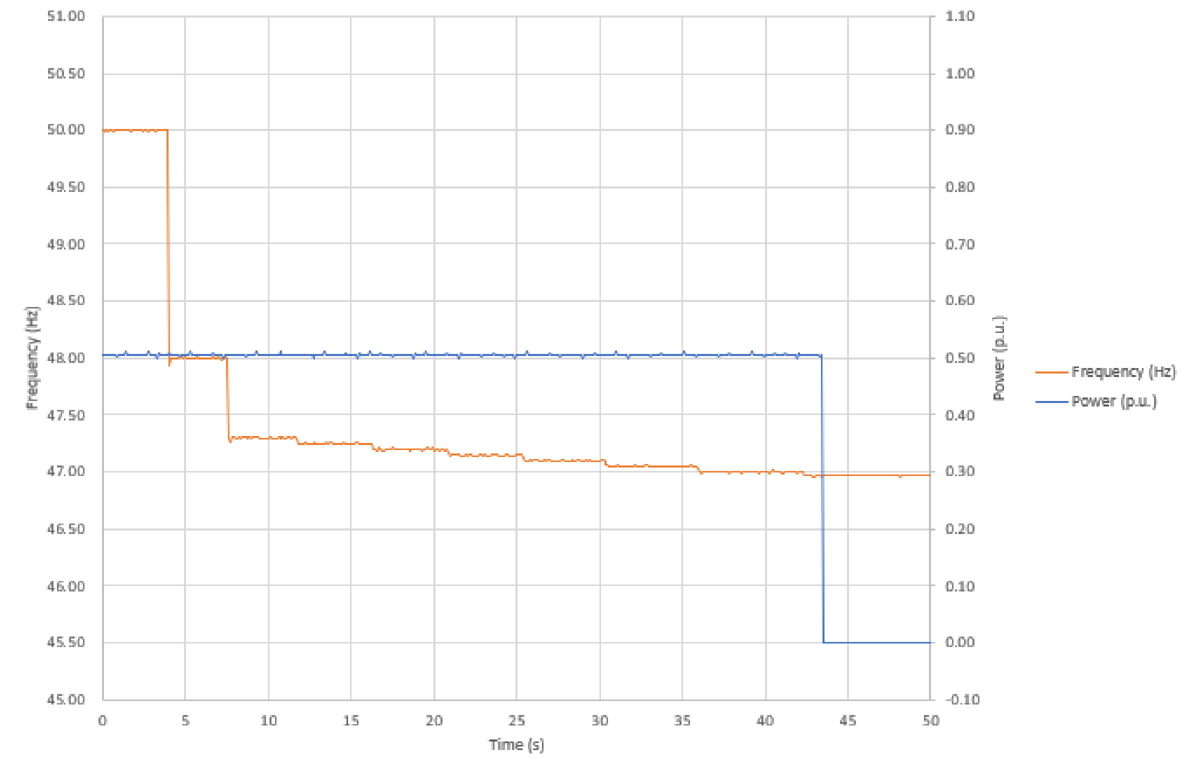
Underfrequency (F<) Rep 1 Australia



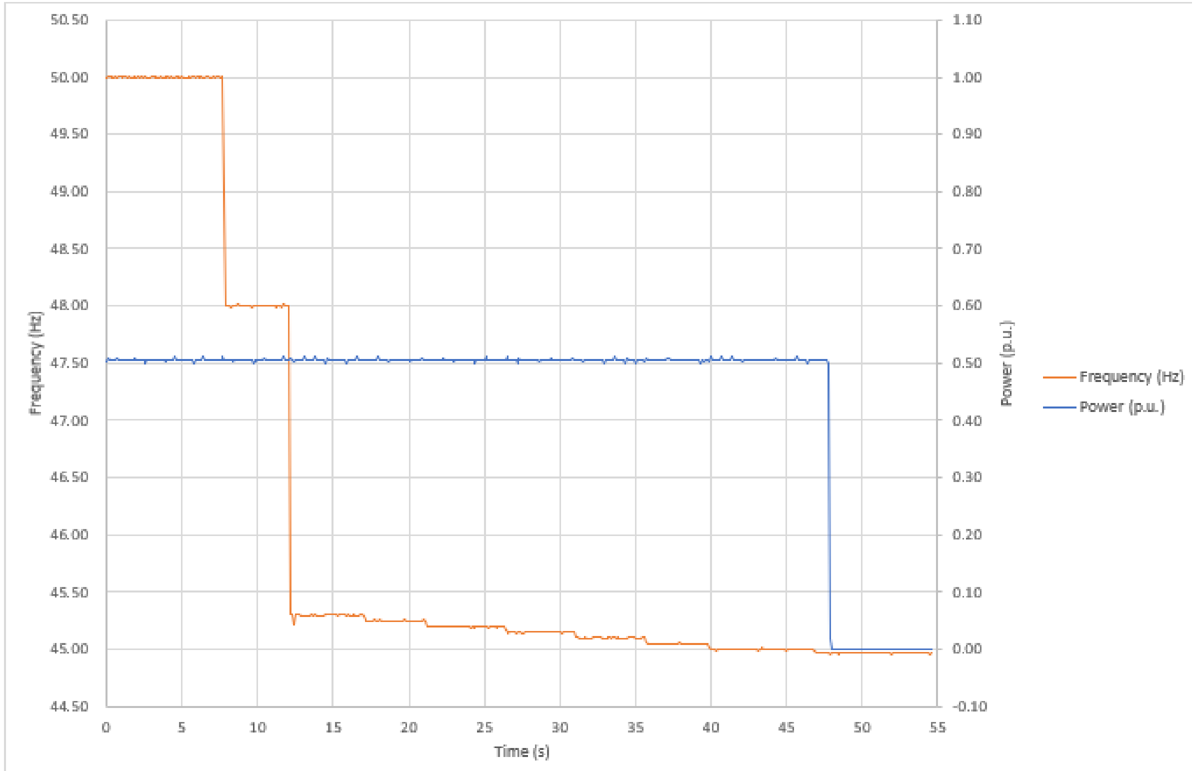
Underfrequency (F<) Rep 2 Australia



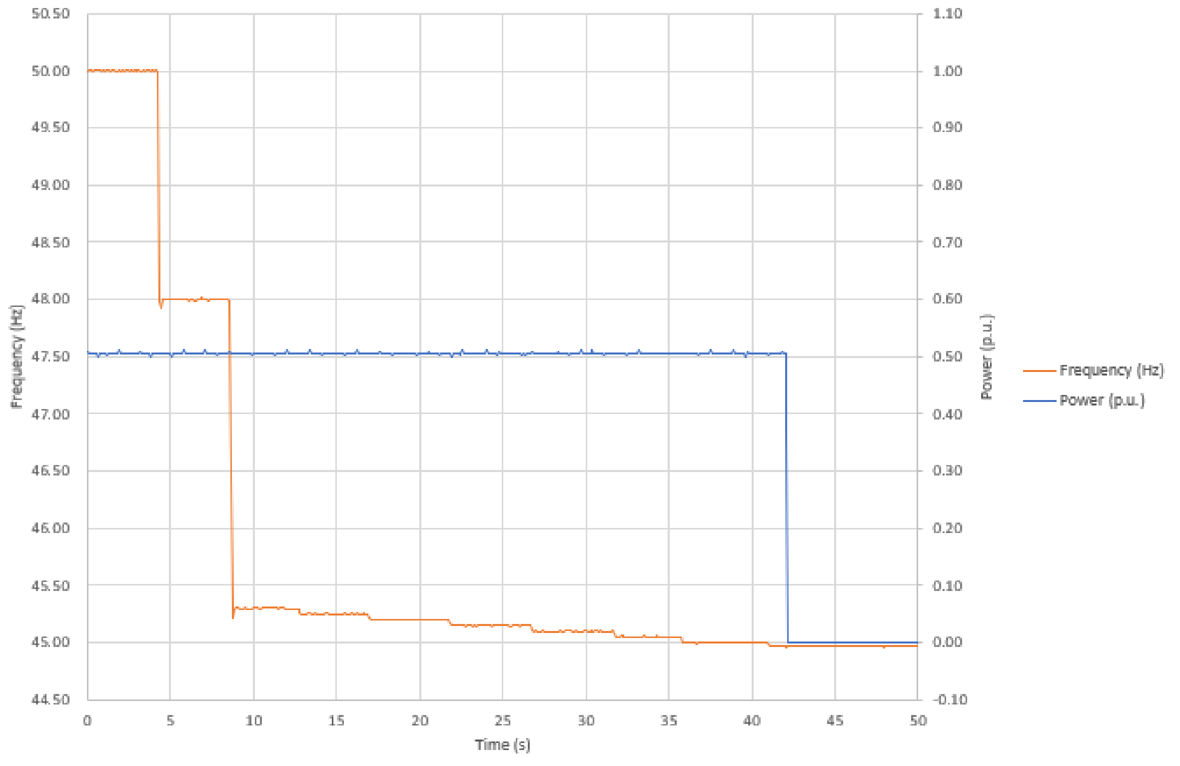
Underfrequency (F<) Rep 3 Australia



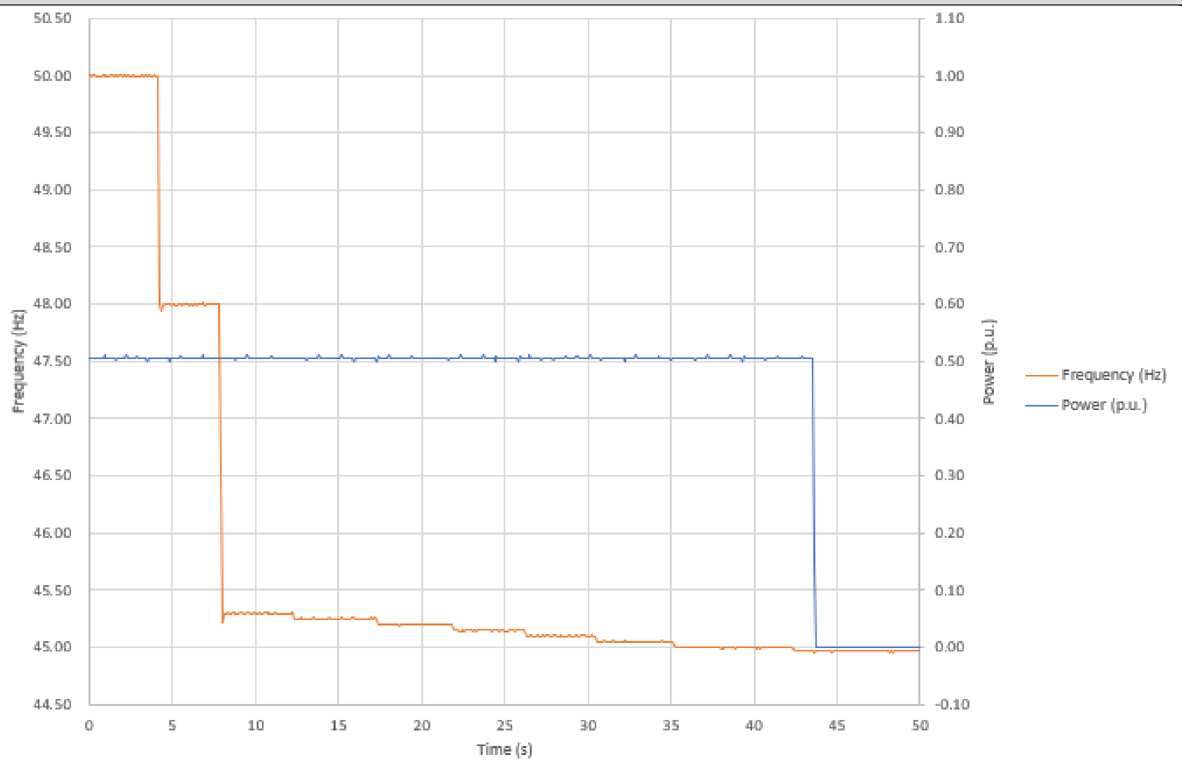
Underfrequency (F<) Rep 1 New Zealand



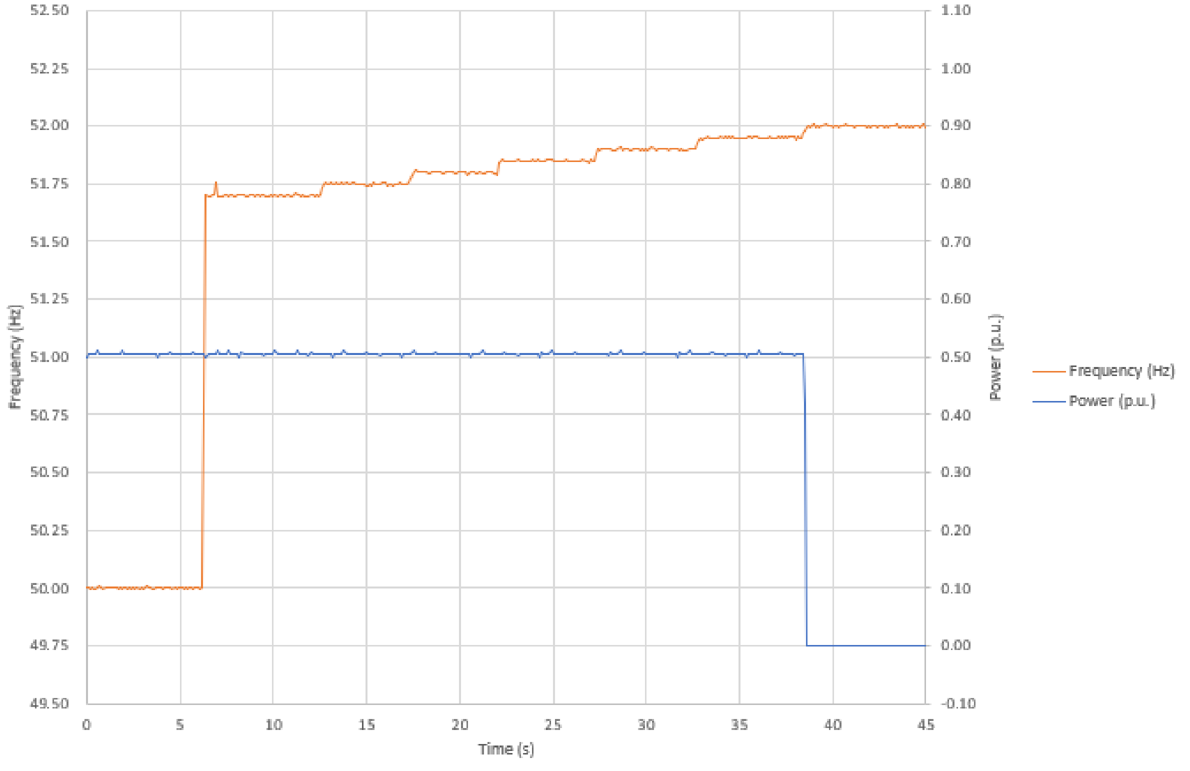
Underfrequency (F<) Rep 2 New Zealand



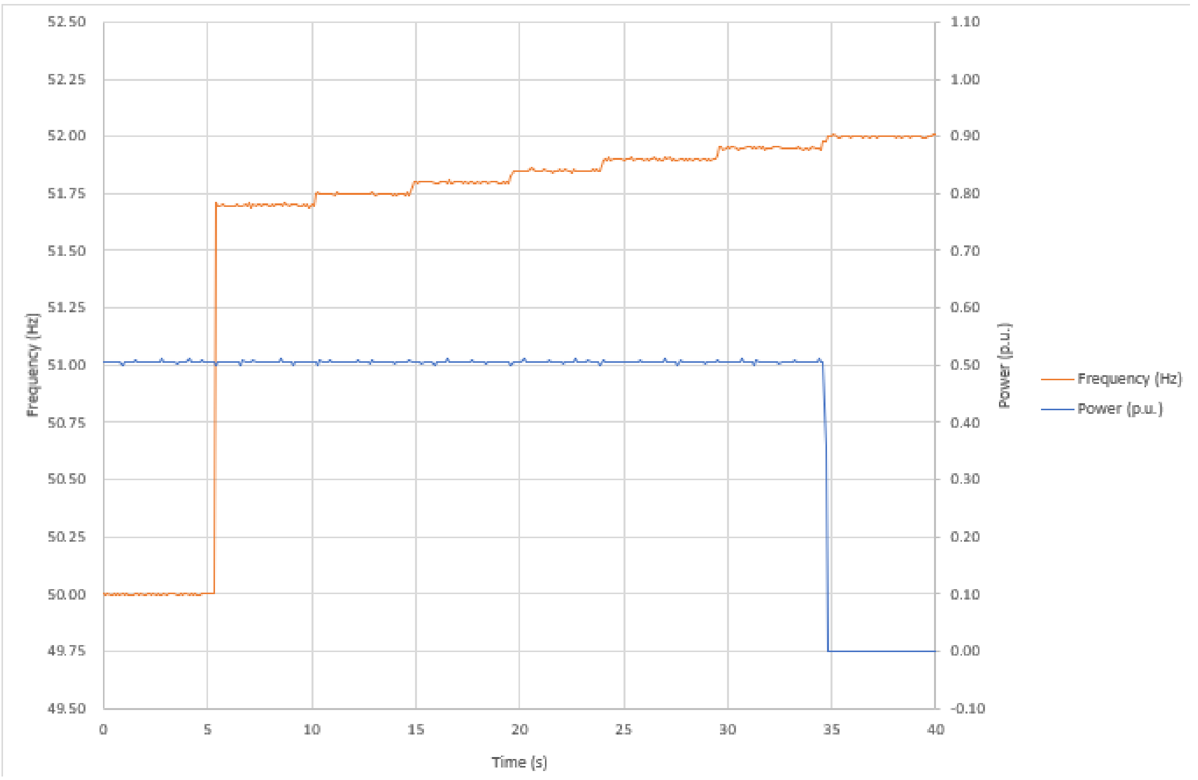
Underfrequency (F<) Rep 3 New Zealand



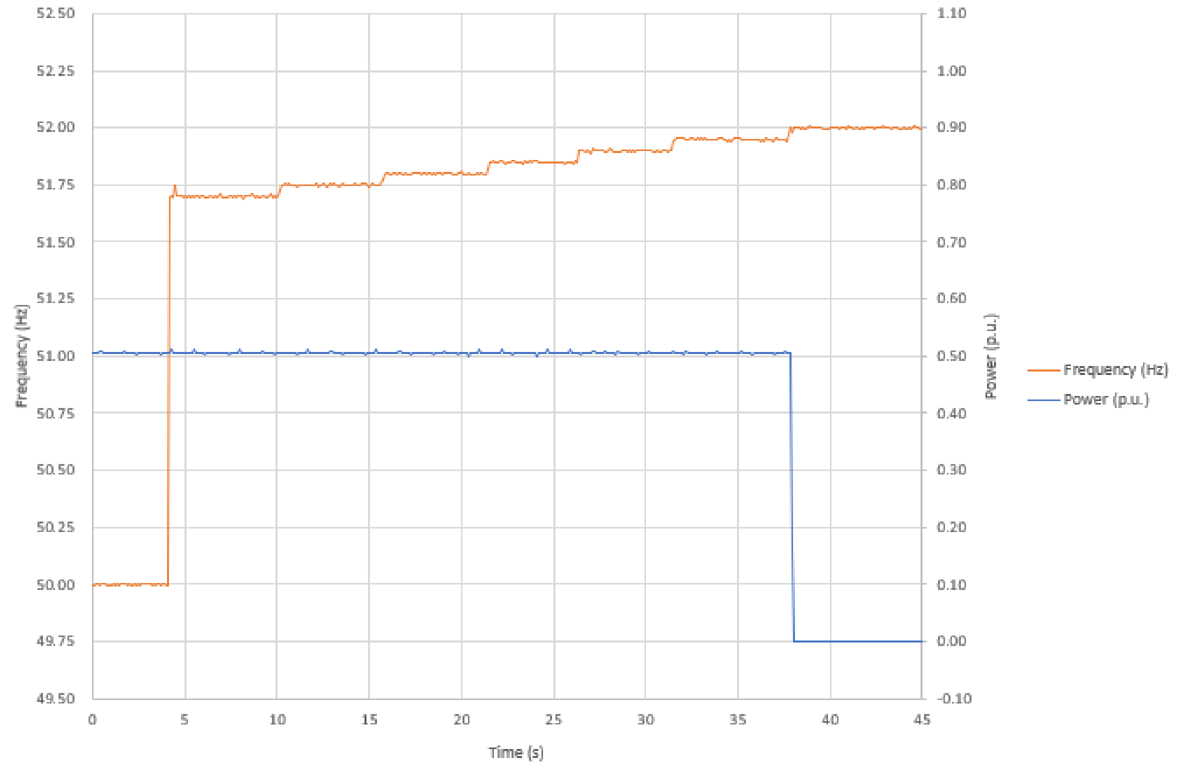
Overfrequency (F>) Rep 1



Overfrequency (F>) Rep 2



Overfrequency (F>) Rep 3



4.18.2.2 Frequency trip time tests

The tests have been made as the following procedure:

- For underfrequency protection: Maintaining the frequency with a value over the settling value during at least 1.5 seconds and then change the frequency to 46 Hz with a step.

- For overfrequency protection: Maintaining the frequency with a value below the settling value during at least 0.5 seconds and then change the frequency to 53 Hz with a step.

For underfrequency the standard states that the trip shall take place with a delay of at least 1 second and in less than 2 seconds, for overfrequency the condition stated by the standard is to trip in less than 0.2 seconds.

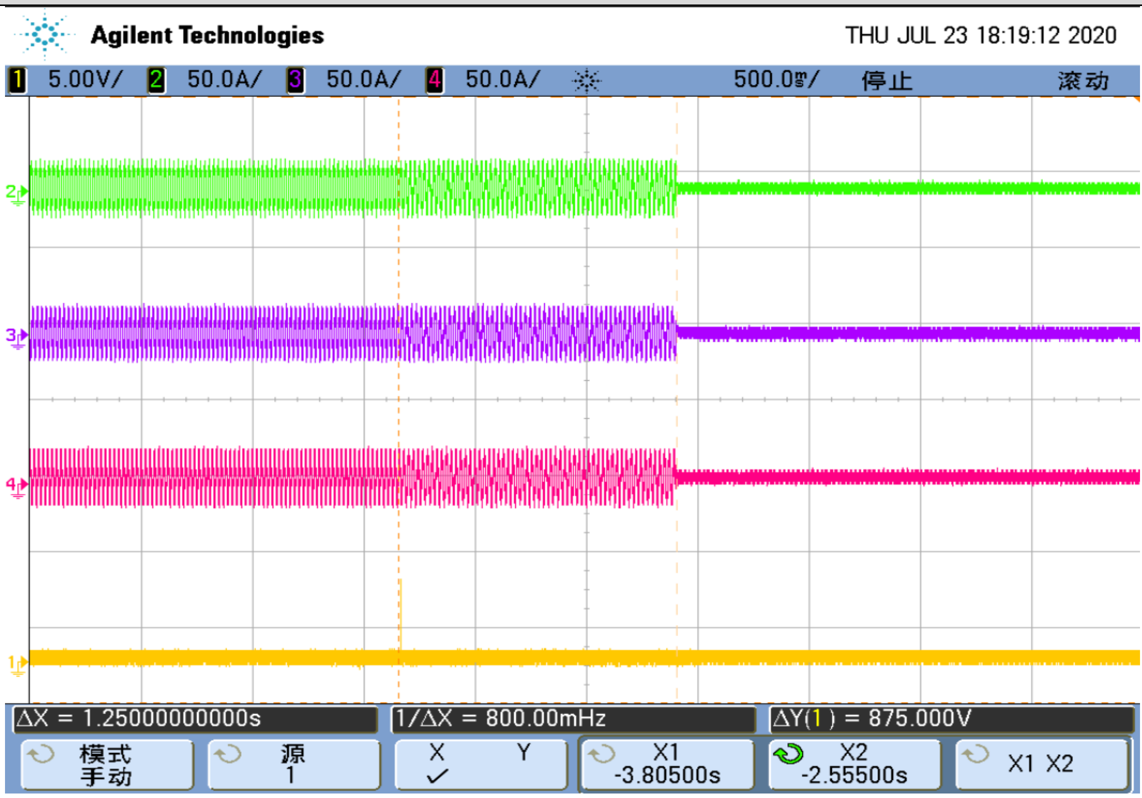
Test results are offered in the following tables:

Protective Function Tested	No Trip Test			Trip Test		
	Frequency value (Hz)	Time measured (s)	Trip	Frequency settling value (Hz)	Trip	Trip Time measured (ms)
F< (Rep1) Australia	47.10	> 1.5	☒ NO ☐ YES	47.00	☐ NO ☒ YES	1250
F< (Rep2) Australia	47.10	> 1.5	☒ NO ☐ YES	47.00	☐ NO ☒ YES	1255
F< (Rep3) Australia	47.10	> 1.5	☒ NO ☐ YES	47.00	☐ NO ☒ YES	1245
F< (Rep1) New Zealand	45.10	> 1.5	☒ NO ☐ YES	45.00	☐ NO ☒ YES	1235
F< (Rep2) New Zealand	45.10	> 1.5	☒ NO ☐ YES	45.00	☐ NO ☒ YES	1270
F< (Rep3) New Zealand	45.10	> 1.5	☒ NO ☐ YES	45.00	☐ NO ☒ YES	1260
F> (Rep 1)	51.90	> 0.5	☒ NO ☐ YES	52.00	☐ NO ☒ YES	127
F> (Rep 2)	51.90	> 0.5	☒ NO ☐ YES	52.00	☐ NO ☒ YES	124
F> (Rep 3)	51.90	> 0.5	☒ NO ☐ YES	52.00	☐ NO ☒ YES	129

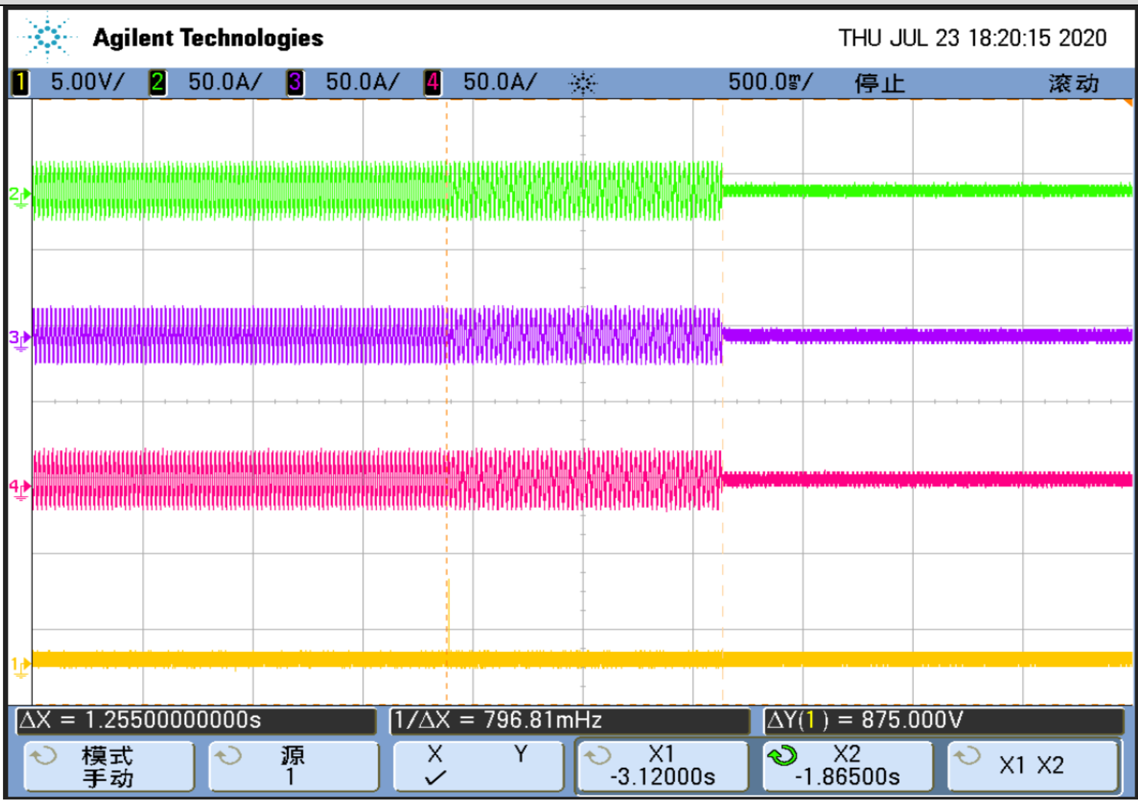
Maximum frequency deviation allowed is ±0.10 Hz.

Test results are graphically shown in following pages.

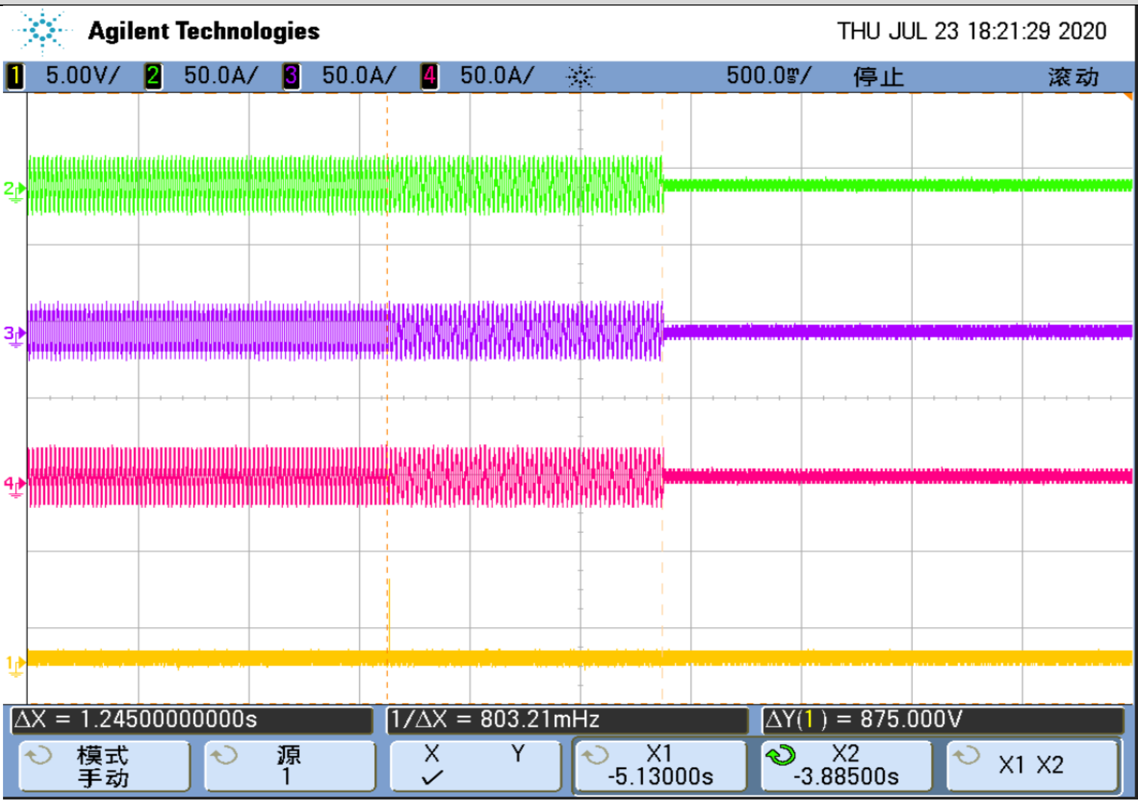
Underfrequency (F<) Rep 1 Australia



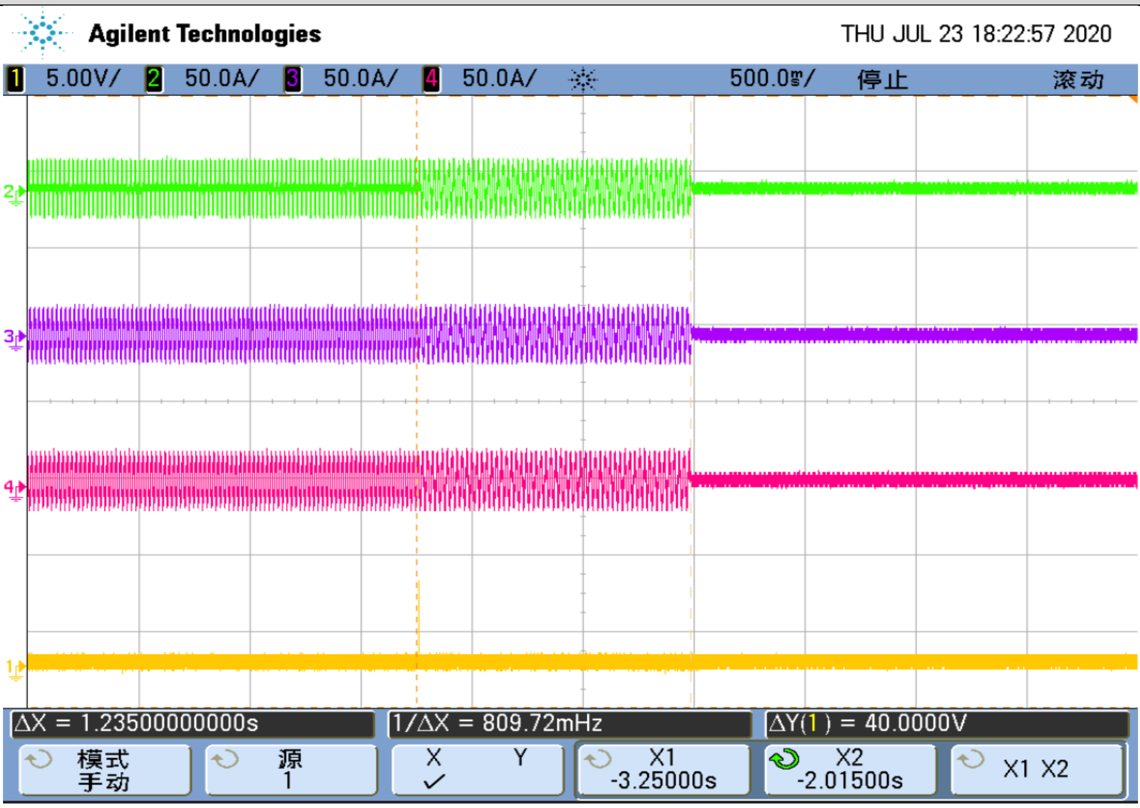
Underfrequency (F<) Rep 2 Australia



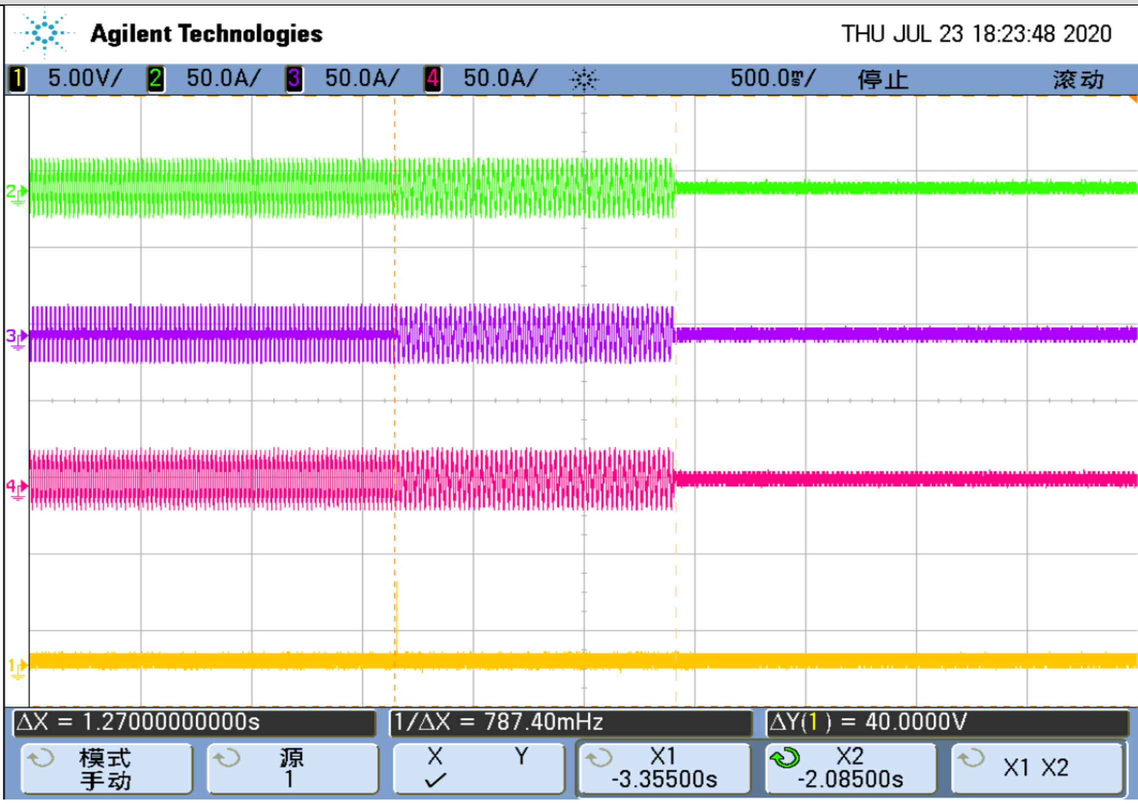
Underfrequency (F<) Rep 3 Australia



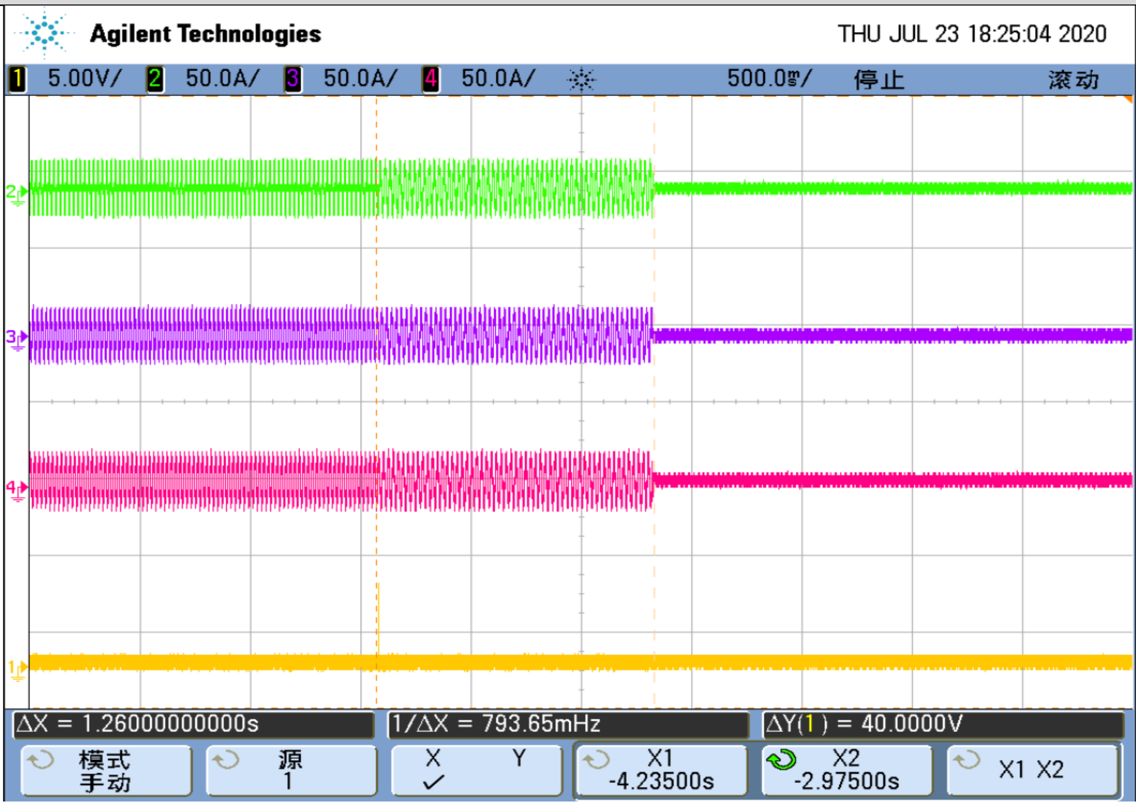
Underfrequency (F<) Rep 1 New Zealand



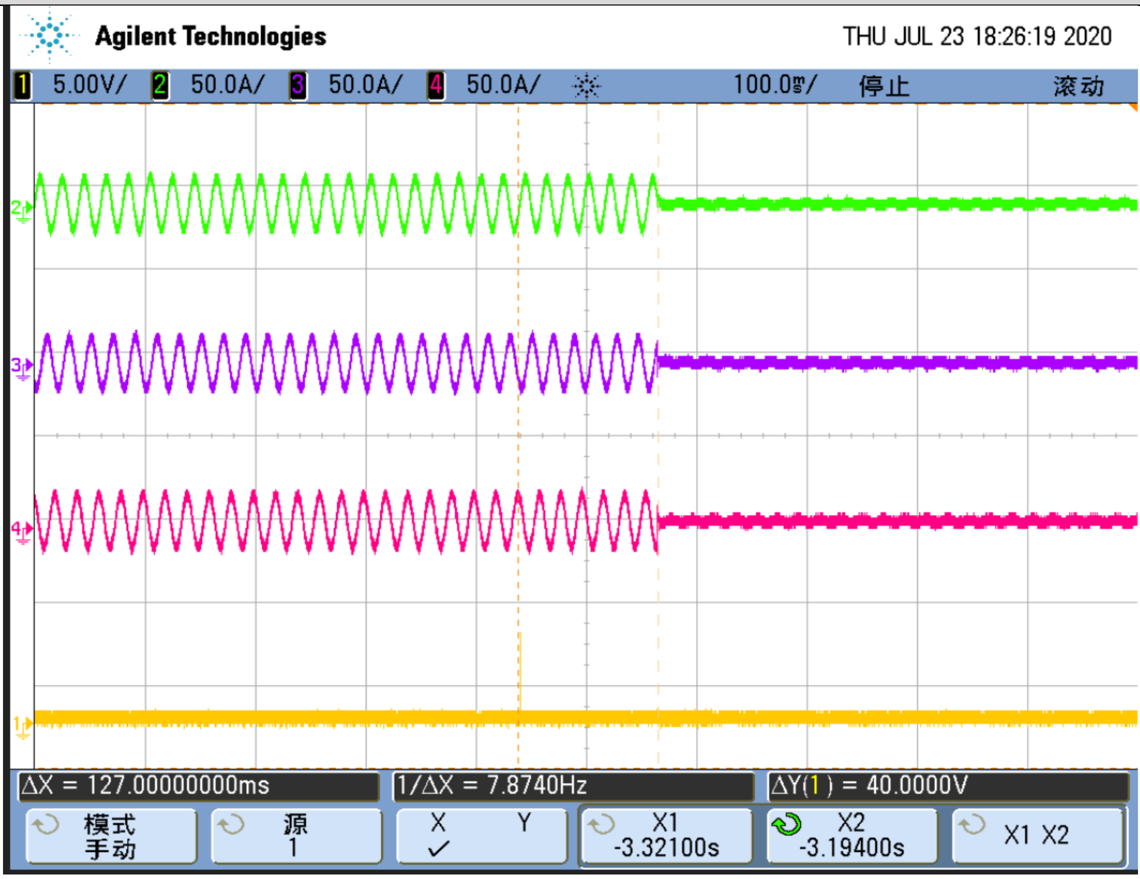
Underfrequency (F<) Rep 2 New Zealand



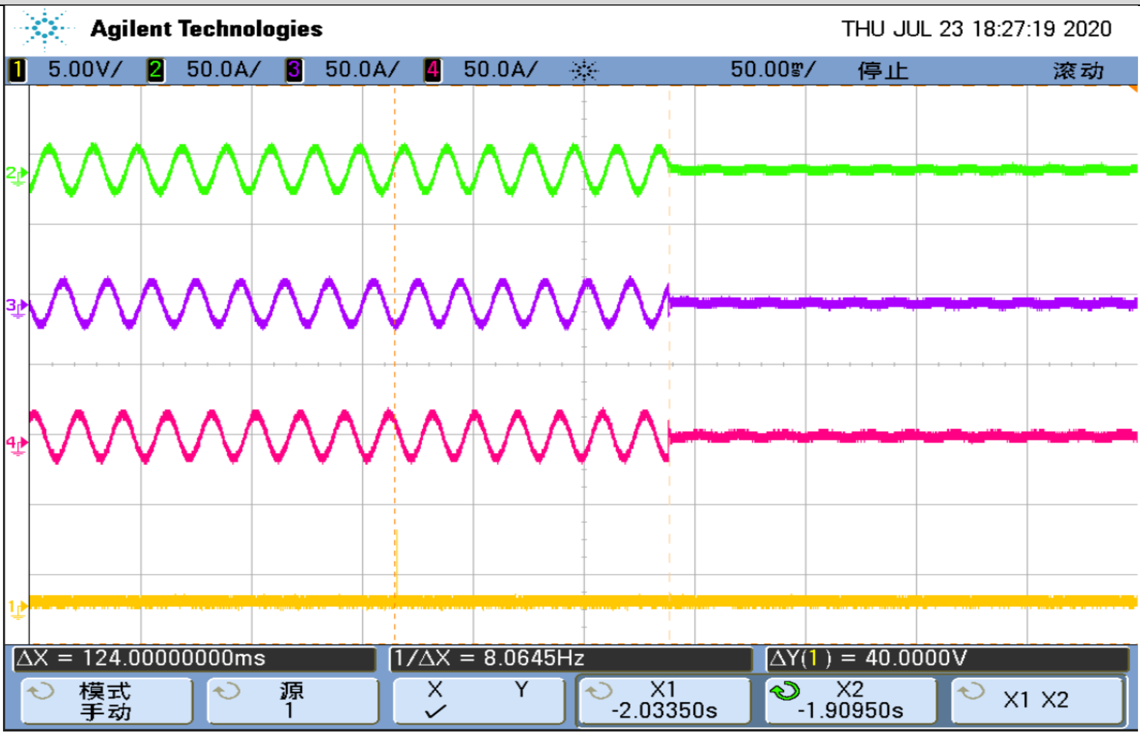
Underfrequency (F<) Rep 3 New Zealand



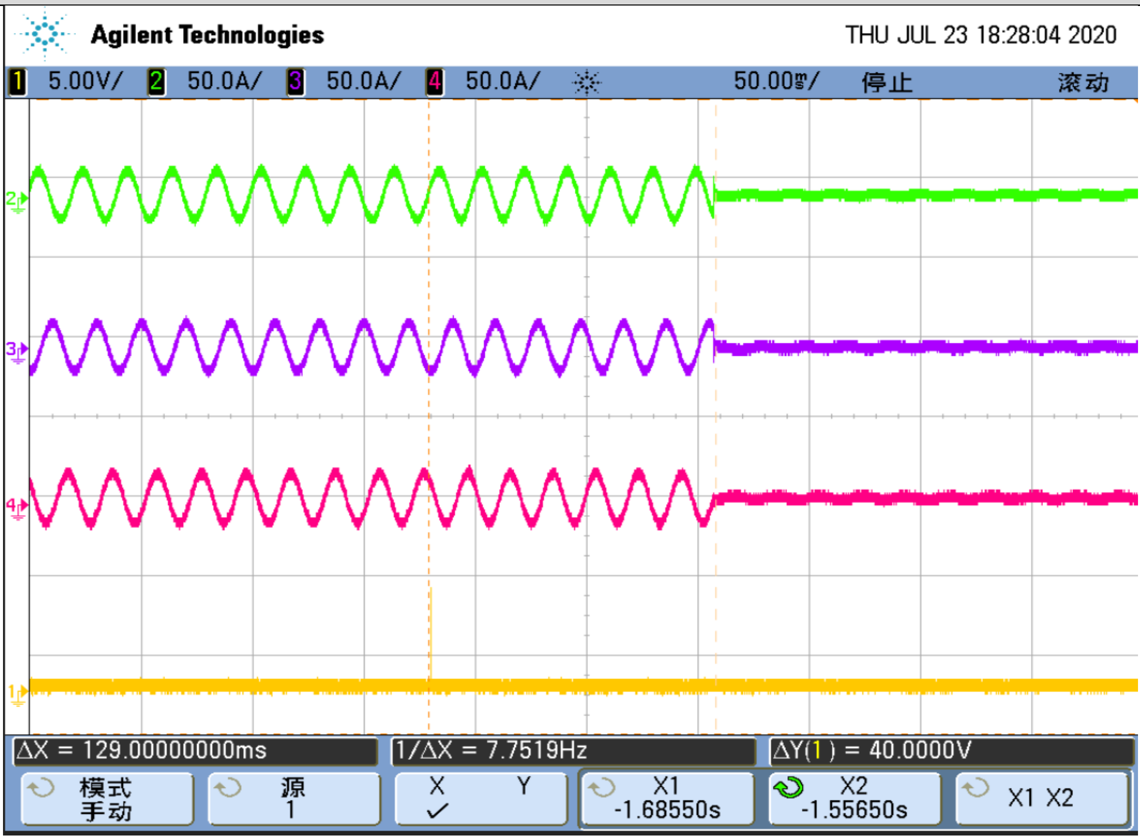
Overfrequency (F>) Rep 1



Overfrequency (F>) Rep 2



Overfrequency (F>) Rep 3



4.19 SUSTAINED OPERATION FOR VOLTAGE VARIATIONS

Tests for verifying the limits sustained operation for voltage variations have been carried out according to the Clause 7.5.2 of the standard.

The inverter shall operate the automatic disconnection device within 3 seconds when the average voltage for a 10 min period exceeds the V_{nom_max}. The voltage value applied for V_{nom_max} is 255V for Australia and 248V for New Zealand.

For the test performed, it has been verified that the inverter trips when any of the calculated voltage averages for total of the three phase system is above Vnom_max.

The test has been repeated 3 times for verifying the accuracy of the voltage trip value and the trip time.

The admissible tolerance between setting value and trip value of the voltage is at maximum set point +/- 1%.

4.19.1 Voltage trip value tests

Starting from a voltage level equal to Un, this voltage is maintained a considerable time verifying that voltage averages calculated in each line are close to Un.

Then, the output voltage is increased up to a voltage equal to the Vnom_max setting less 1V. This level is maintained for 5 minutes.

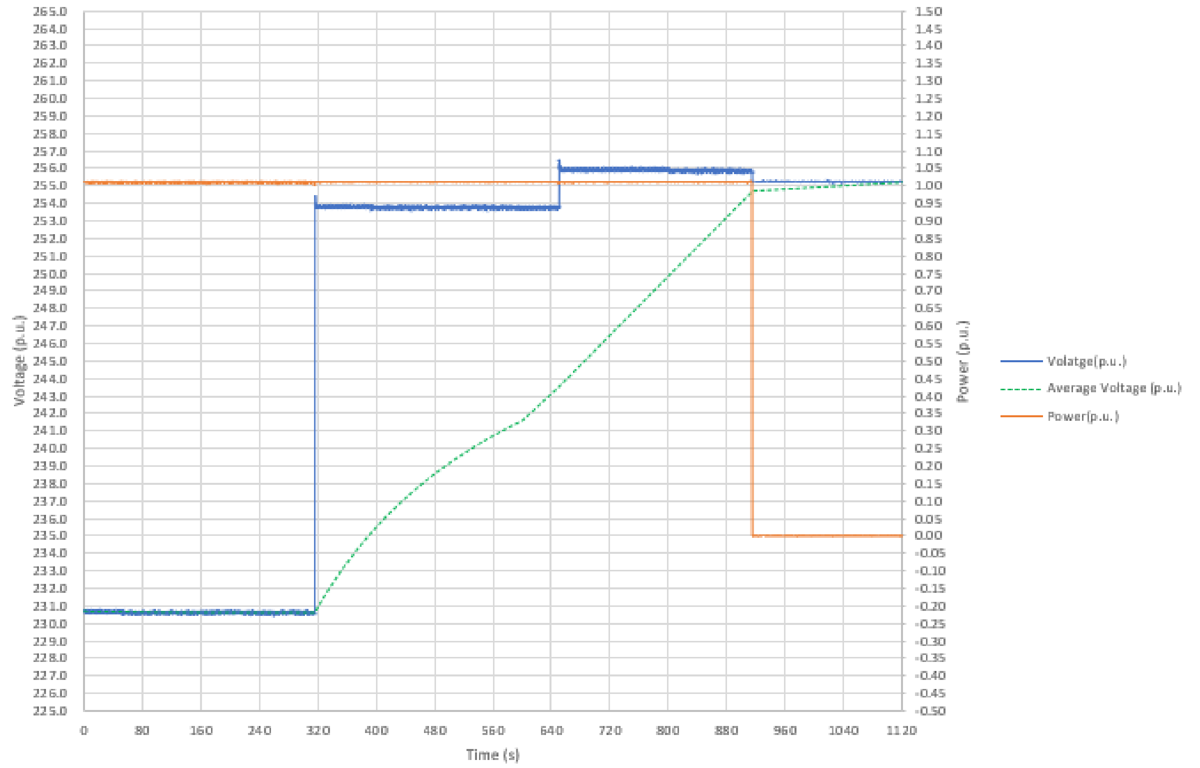
After this, the output voltage is increased up to a voltage equal to the Vnom_max setting plus 1V. This level is maintained up to the inverter trips and the voltage average value is recorded.

The table below offers test results obtained. Where the test procedure above mentioned has been applied.

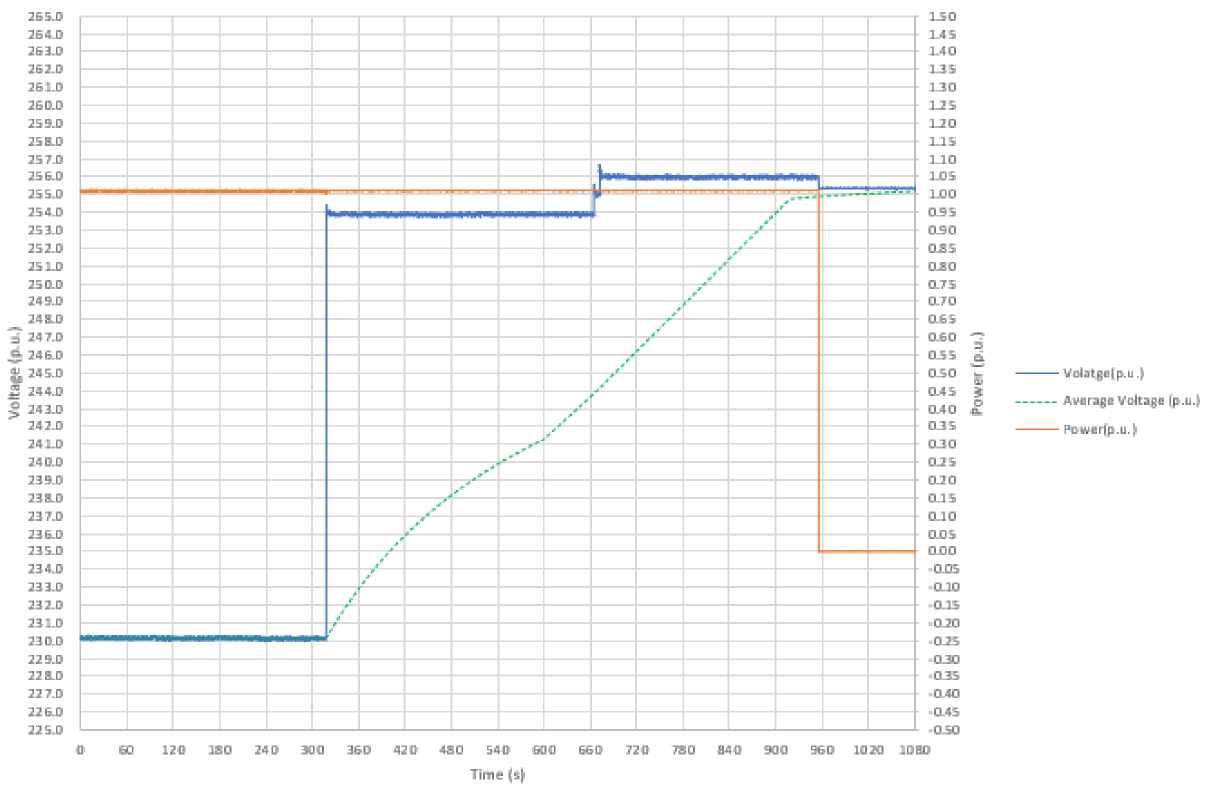
Test number	Threshold Value (V)	No Trip Test			Trip Test		
		Voltage value (V)	Time measured (s)	Trip	Voltage settling value (V)	Trip	Trip voltage average value (V)
Setting according to AS 60038 for Australia							
1	255.0	254.0	> 300	☒ NO ☐ YES	256.0	☐ NO ☒ YES	254.7
2	255.0	254.0	> 300	☒ NO ☐ YES	256.0	☐ NO ☒ YES	254.9
3	255.0	254.0	> 300	☒ NO ☐ YES	256.0	☐ NO ☒ YES	255.0
Setting according to IEC 60038 for New Zealand							
1	248.0	247.0	> 300	☒ NO ☐ YES	249.0	☐ NO ☒ YES	247.9
2	248.0	247.0	> 300	☒ NO ☐ YES	249.0	☐ NO ☒ YES	247.9
3	248.0	247.0	> 300	☒ NO ☐ YES	249.0	☐ NO ☒ YES	248.0

After these test results, it is considered the most restrictive trip voltage average value for verifying the trip time. With this,

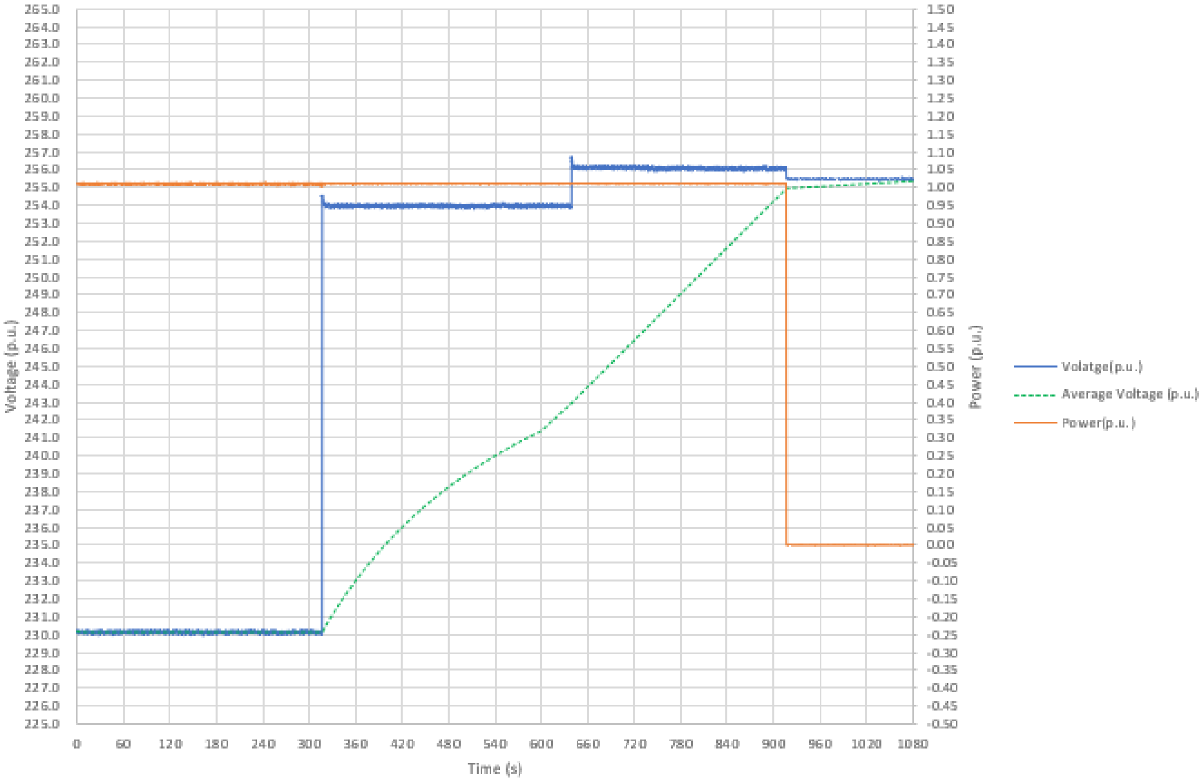
Sustained operation for Voltage Variations setting at 255V (Test 1: voltage average trip value test)



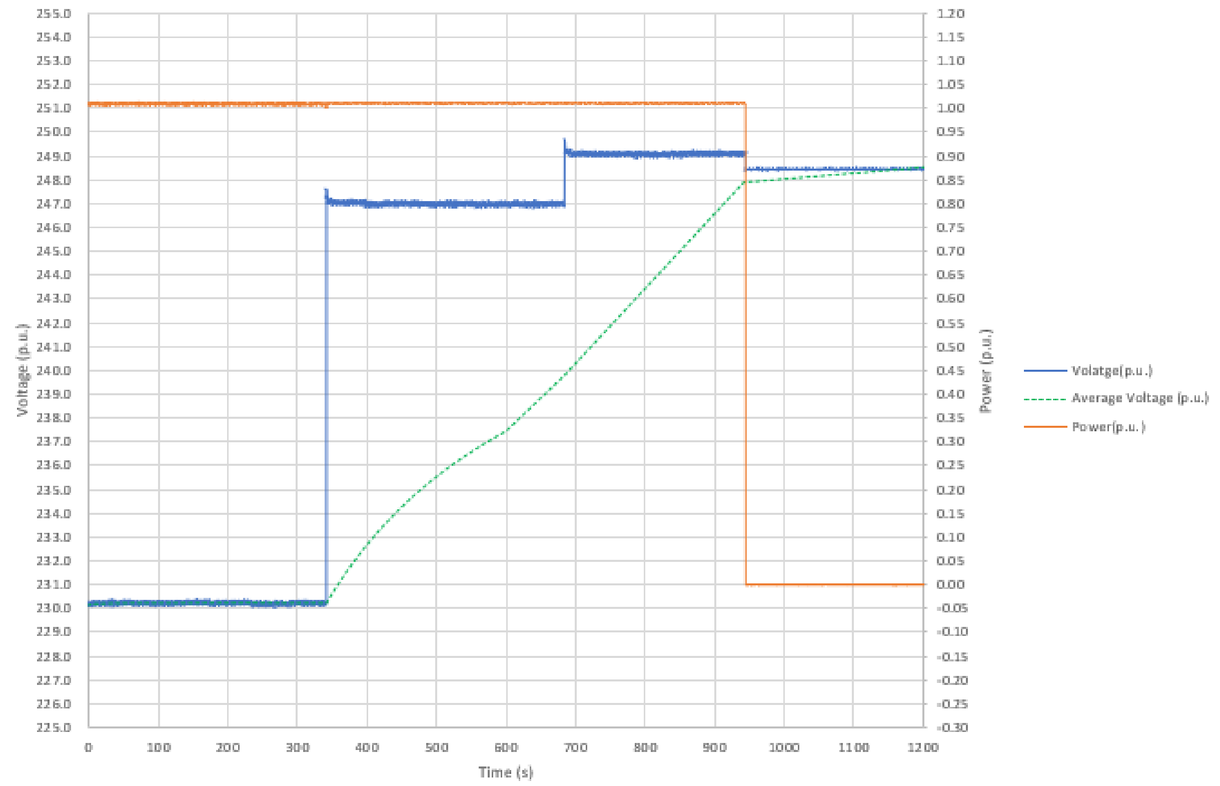
Sustained operation for Voltage Variations setting at 255V (Test 2: voltage average trip value test)



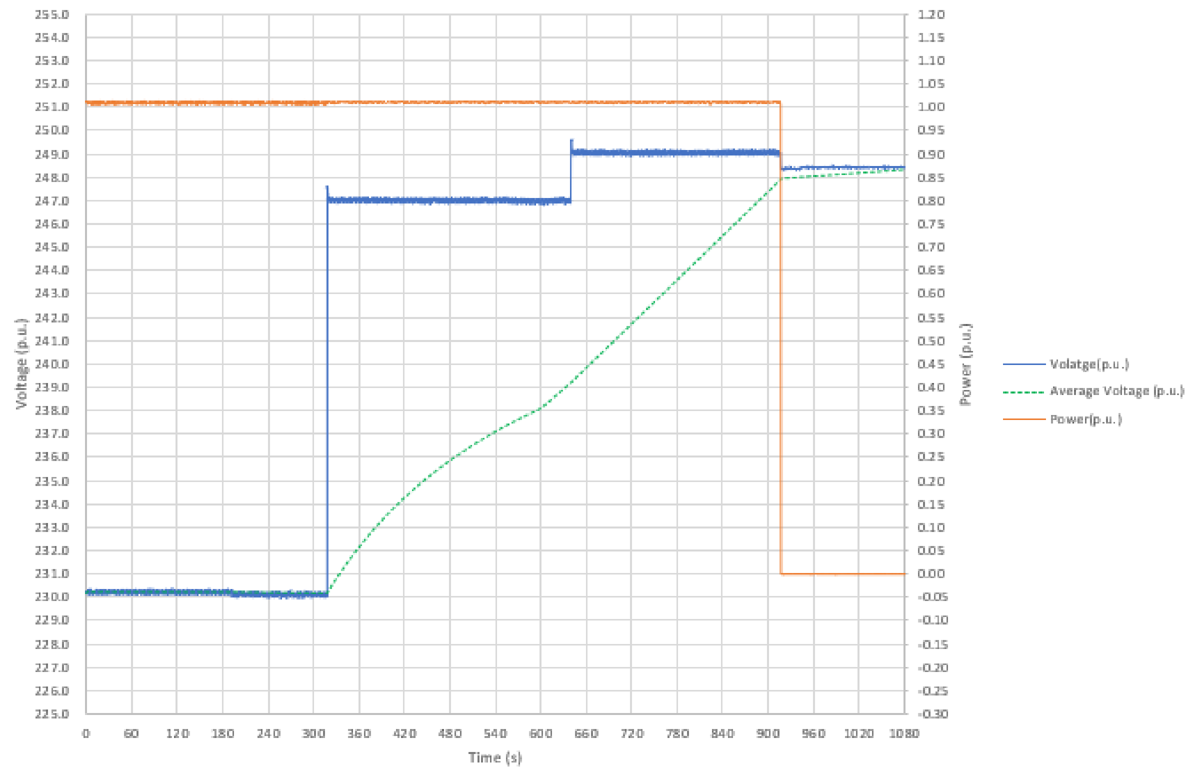
Sustained operation for Voltage Variations setting at 255V
(Test 3: voltage average trip value test)



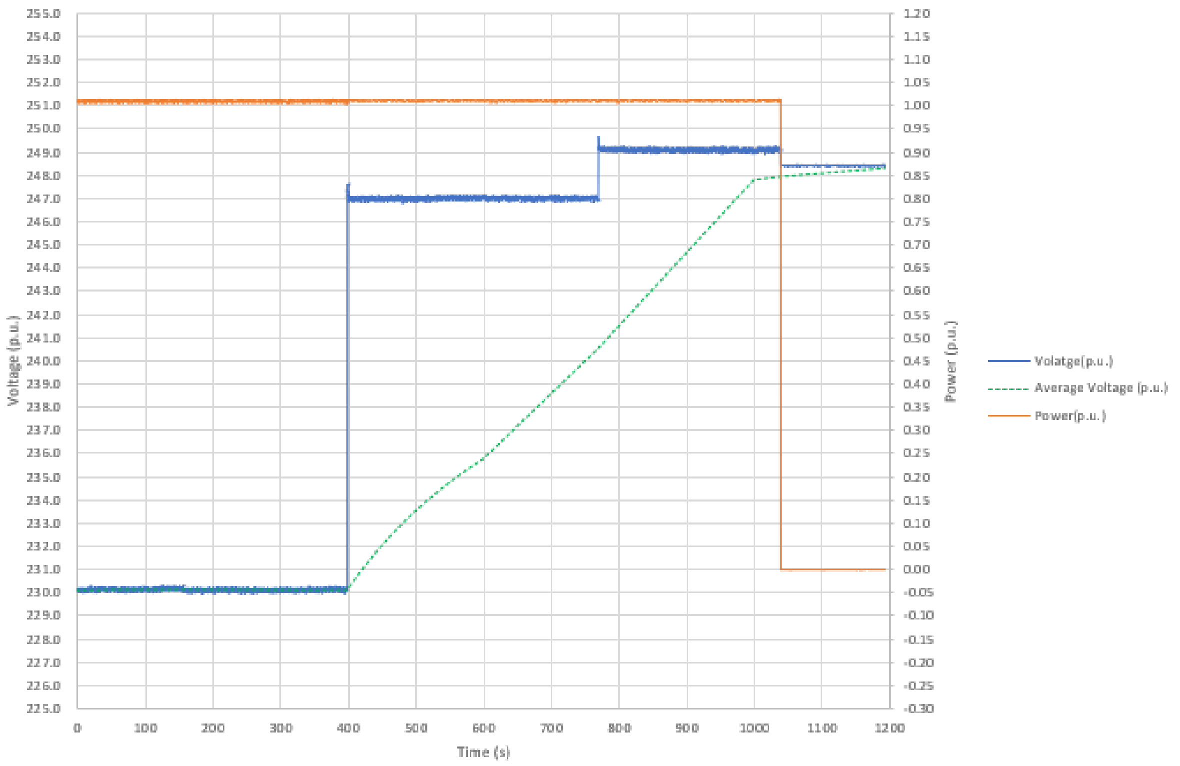
Sustained operation for Voltage Variations setting at 248V (Test 1: voltage average trip value test)



Sustained operation for Voltage Variations setting at 248V (Test 2: voltage average trip value test)



Sustained operation for Voltage Variations setting at 248V
(Test 3: voltage average trip value test)



4.19.2 Trip time test

Starting from a voltage level equal to Un, this voltage is maintained a considerable time verifying that voltage averages calculated in each line are close to Un.

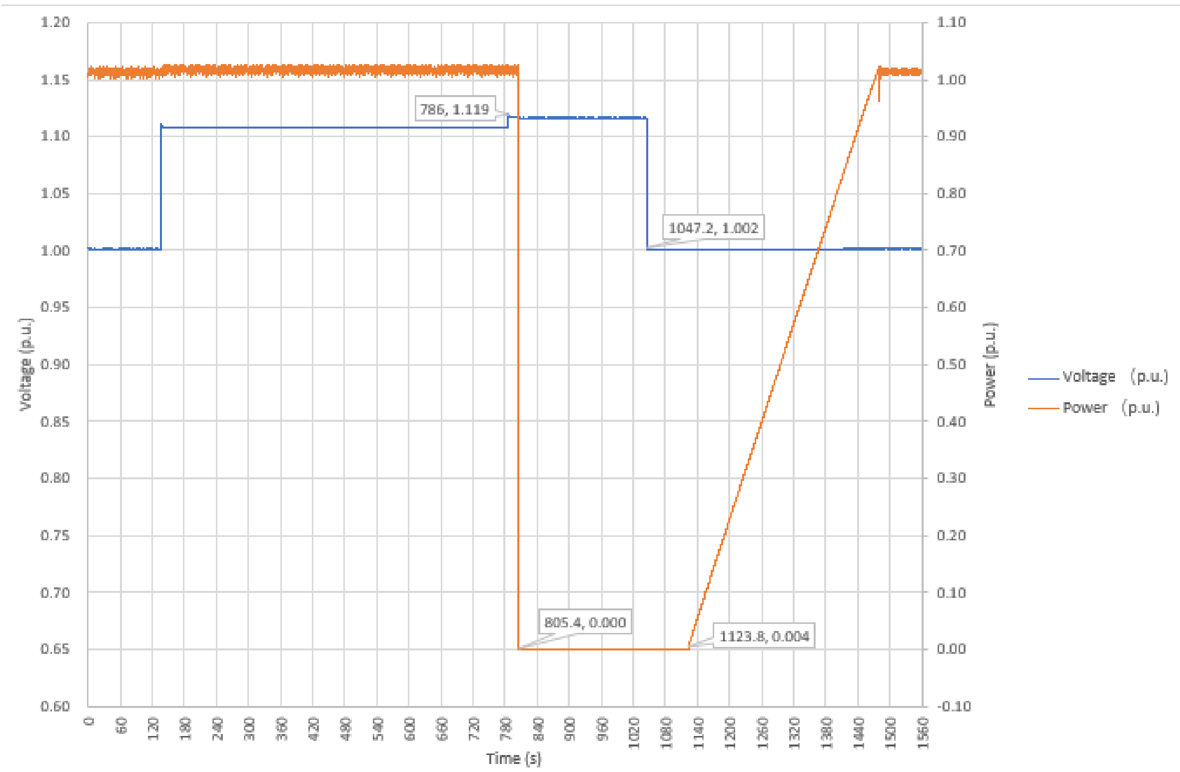
Then, the output voltage is increased up to a voltage equal to the Vnom_max setting calculated after the test 1. This level is maintained for 10 minutes.

After this, the output voltage is increased up to a voltage equal to the Vnom_max setting plus 2V. This level is maintained up to the inverter trips and the voltage average value is recorded. This trip time shall be less than 30 seconds.

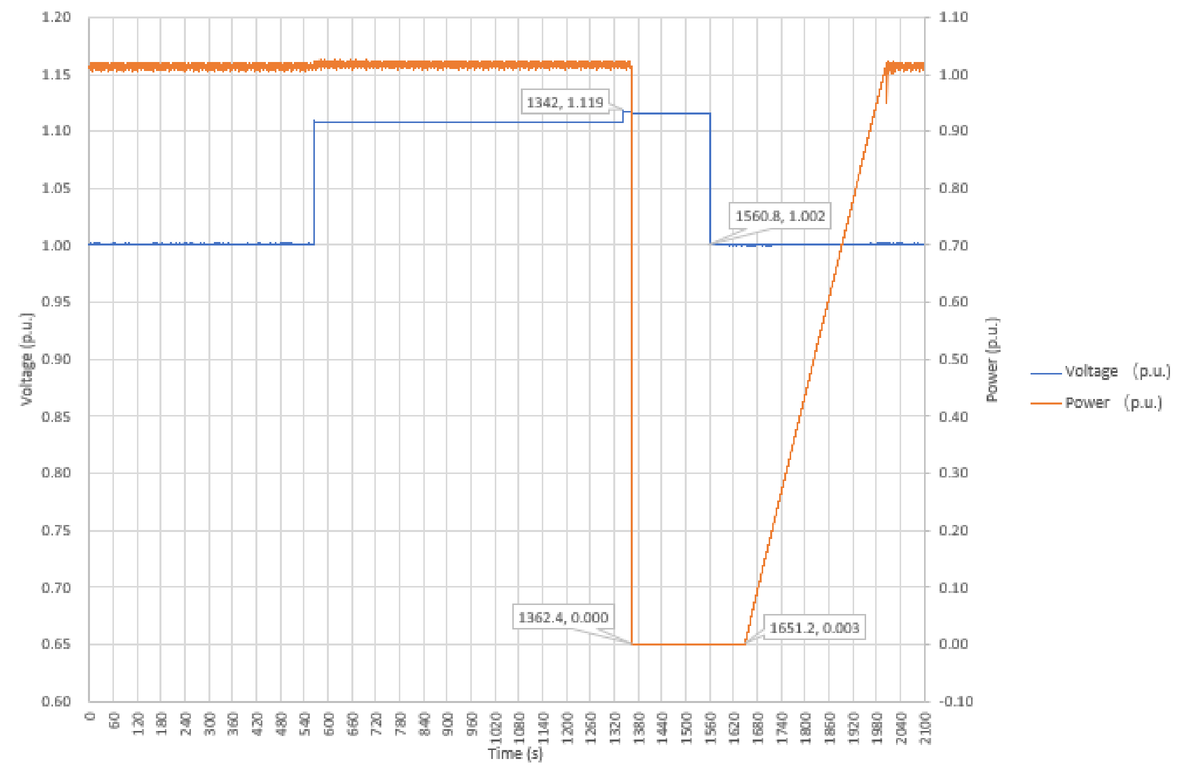
The table below offers test results obtained, where the test procedure above mentioned has been applied.

Threshold Value (V)	No Trip Test			Trip Test		
	Voltage value (V)	Time measured (s)	Trip	Voltage value (%Un)	Trip	Measured Trip time (s)
Setting according to AS 60038 for Australia						
255	254.8	> 600	☒ NO ☐ YES	256.8	☐ NO ☒ YES	19.4
255	254.8	> 600	☒ NO ☐ YES	256.6	☐ NO ☒ YES	20.4
255	254.8	> 600	☒ NO ☐ YES	256.6	☐ NO ☒ YES	22.2
Setting according to IEC 60038 for New Zealand						
248	247.8	> 600	☒ NO ☐ YES	249.3	☐ NO ☒ YES	22.2
248	247.8	> 600	☒ NO ☐ YES	249.3	☐ NO ☒ YES	21.0
248	247.8	> 600	☒ NO ☐ YES	249.3	☐ NO ☒ YES	23.2

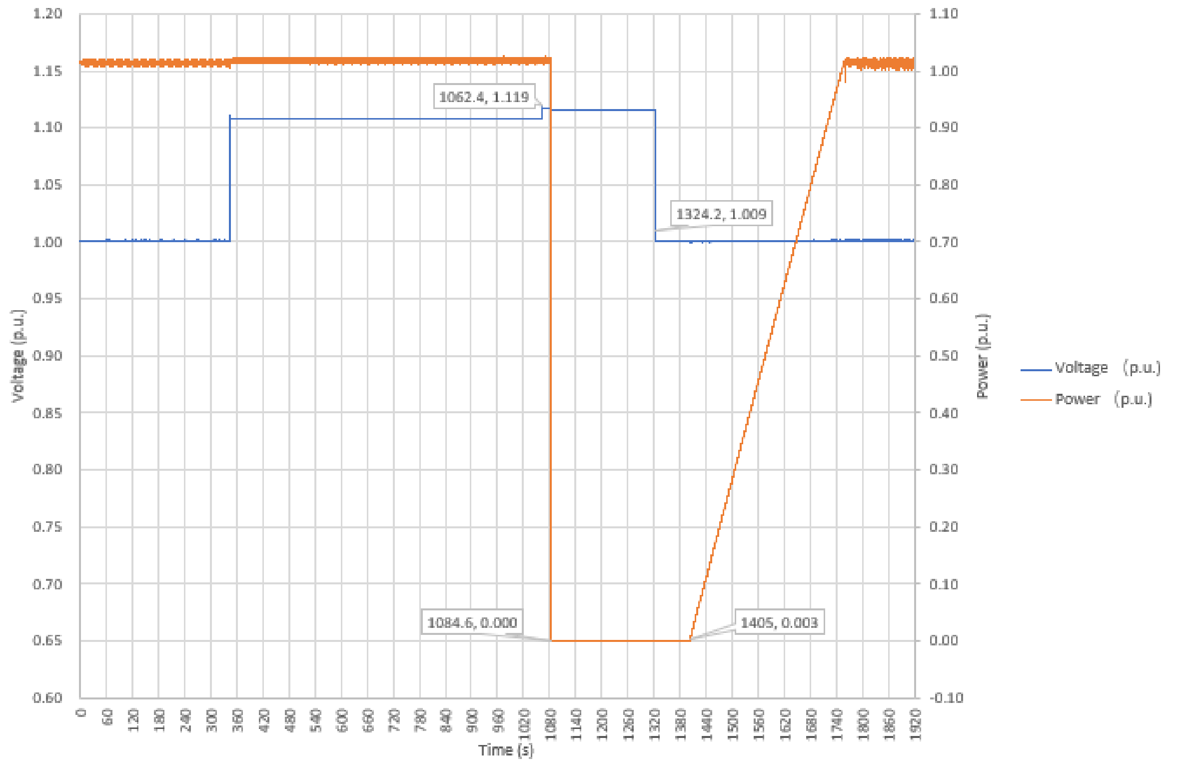
Sustained operation for Voltage Variations setting at 255V (trip time test)



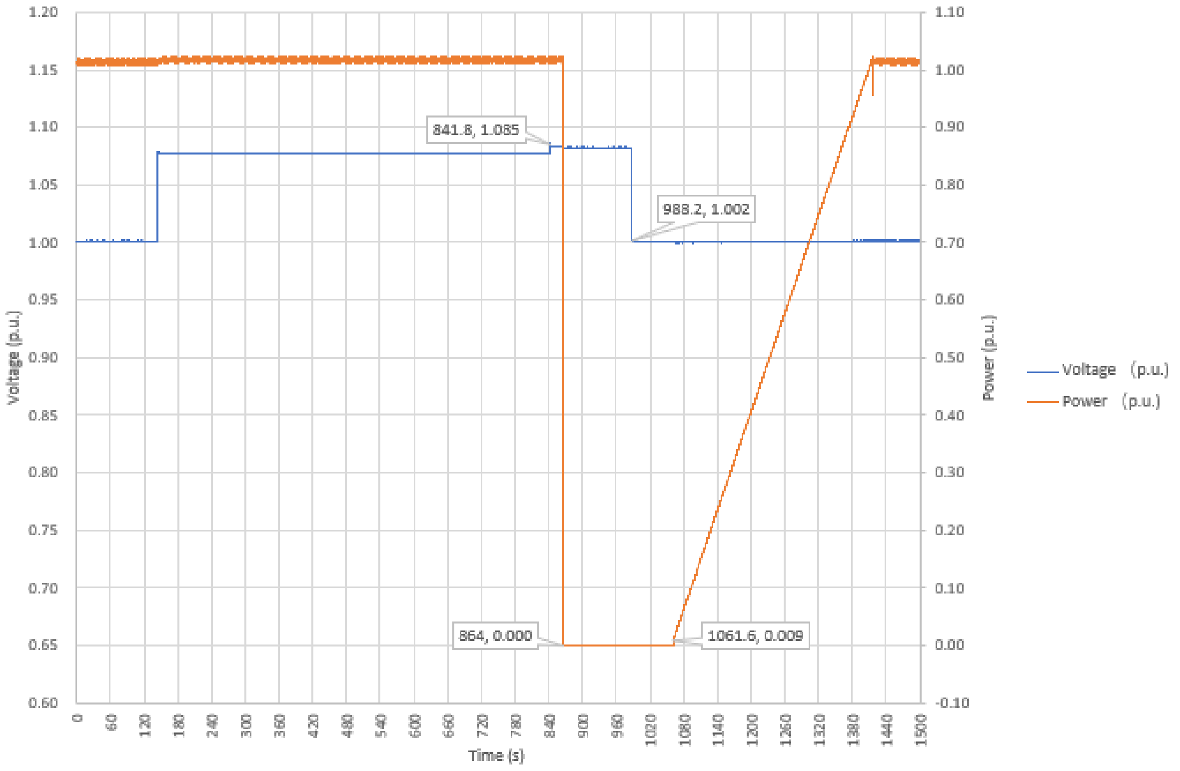
Sustained operation for Voltage Variations setting at 255V (trip time test)



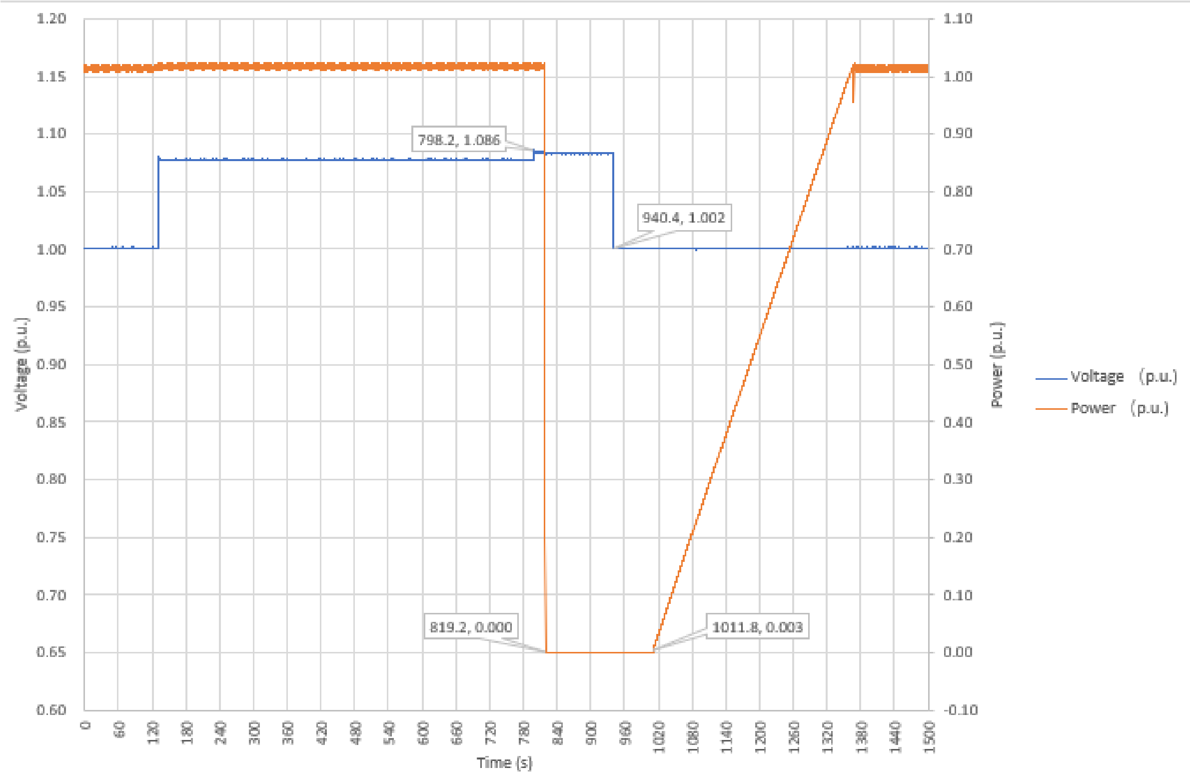
Sustained operation for Voltage Variations setting at 255V (trip time test)



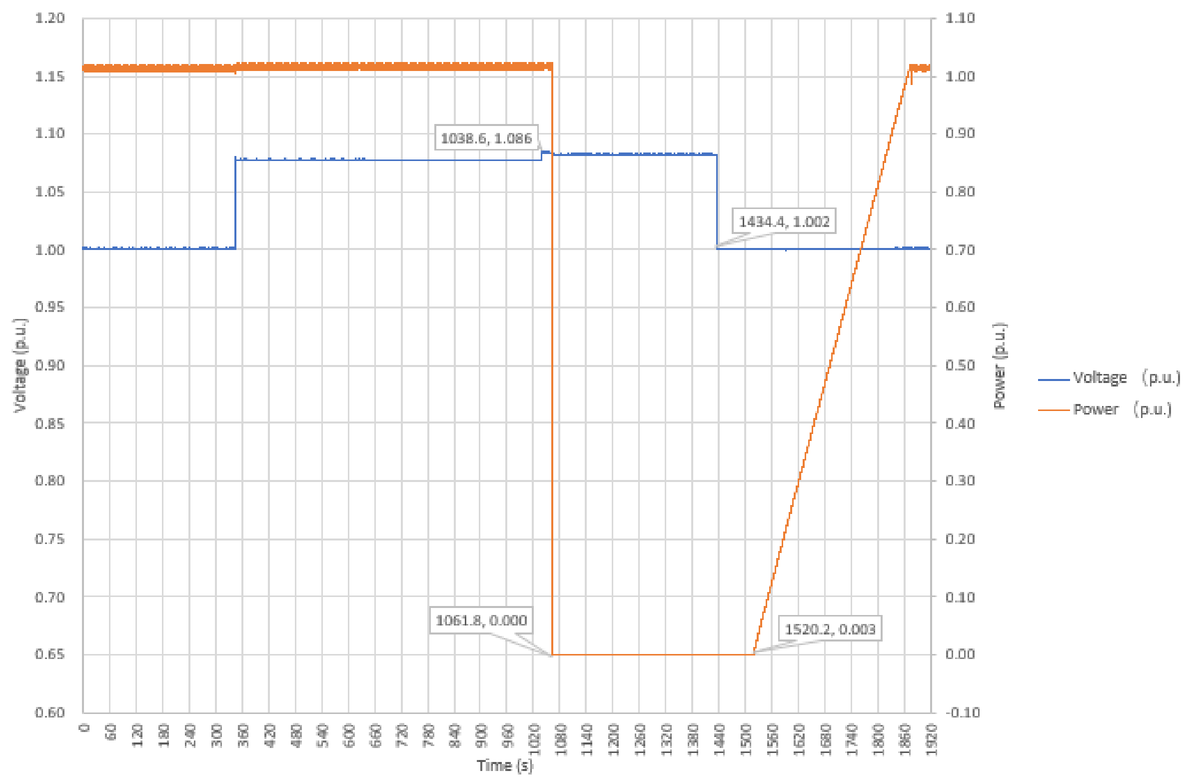
Sustained operation for Voltage Variations setting at 248V (trip time test)



Sustained operation for Voltage Variations setting at 248V (trip time test)



Sustained operation for Voltage Variations setting at 248V (trip time test)



4.20 SUSTAINED OPERATION FOR FREQUENCY VARIATIONS

Sustained operation for frequency variations has been measured according to the Clause 7.5.3 of the standard.

4.20.1 Response to an increase in frequency

According to the clause 7.5.3.1 the inverter must be able to comply with the following requirements:

- Test 1: Linear decrease of the active power up to disconnection in front of over frequency variations up to 52 Hz.
- Test 2: Hysteresis capability once over frequency variations are recovered up to 50.15Hz.

When the inverter's frequency returns to operate with f < 50.15 Hz, the active power must be recovered in both cases according to a power ramp limit and with a delay of at least 60 seconds.

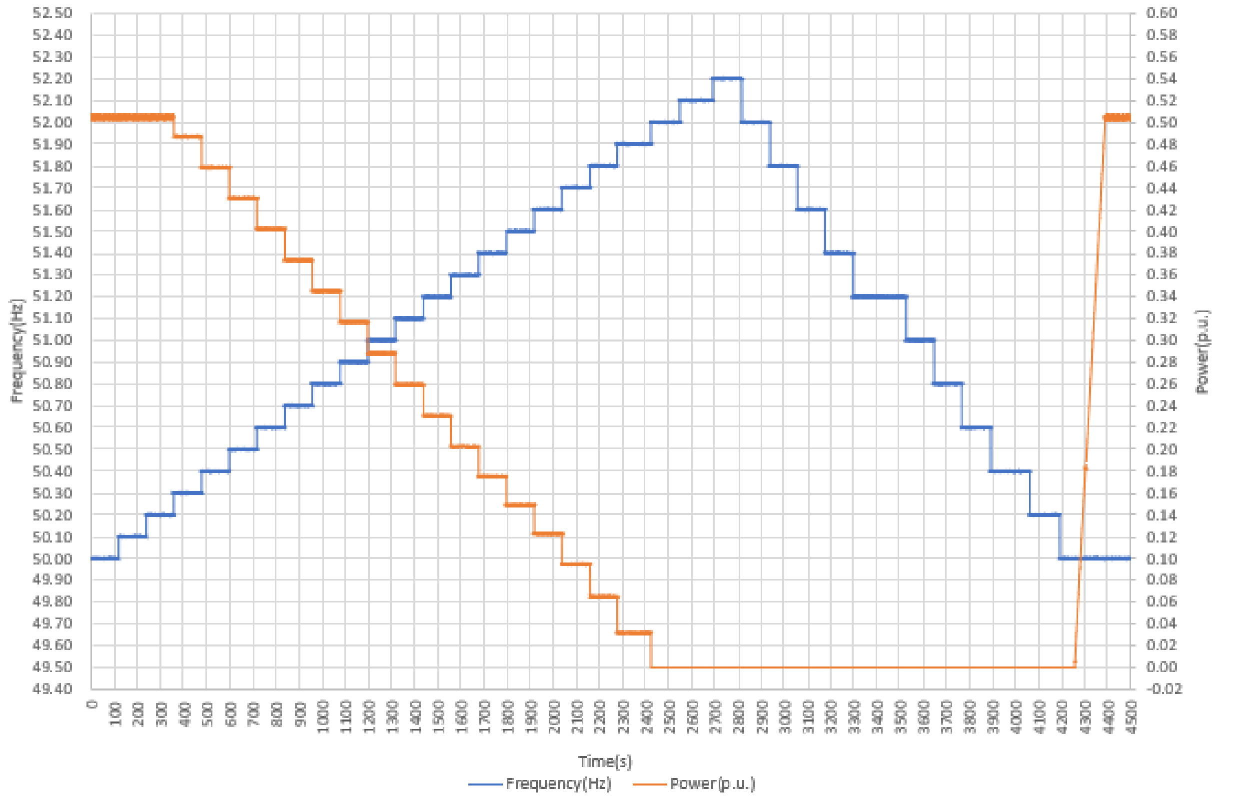
Test results obtained are shown in the following tables and graphs.

Test 1. Over frequency variations up to disconnection and active power recovery				
%Pn	**Frequency (Hz)**	**Power measured (W)**	**Power desired (W)**	**ΔP (%P_M)**
50 %	50.00	7568	7500	0.91
	50.10	7568	7500	0.91
	50.20	7571	7500	0.95
	50.30	7301	7286	0.20
	50.40	6876	6857	0.25
	50.50	6451	6429	0.30
	50.60	6028	6000	0.37
	50.70	5604	5571	0.43
	50.80	5178	5143	0.47
	50.90	4750	4714	0.48
	51.00	4321	4286	0.47
	51.10	3890	3857	0.44
	51.20	3460	3429	0.42
	51.30	3035	3000	0.47
	51.40	2628	2571	0.75
	51.50	2230	2143	1.16
	51.60	1838	1714	1.65
	51.70	1420	1286	1.79
	51.80	973	857	1.54
	51.90	473	429	0.59
	52.00	-1	0	-0.01
	52.10	-1	0	-0.01
	52.20	-1	0	-0.01
	52.00	-1	0	-0.01
	51.80	-1	0	-0.01
	51.60	-1	0	-0.01
	51.40	-1	0	-0.01
	51.20	-1	0	-0.01
	51.00	-1	0	-0.01
	50.80	-1	0	-0.01
	50.60	-1	0	-0.01
	50.40	-1	0	-0.01
	50.20	-1	0	-0.01

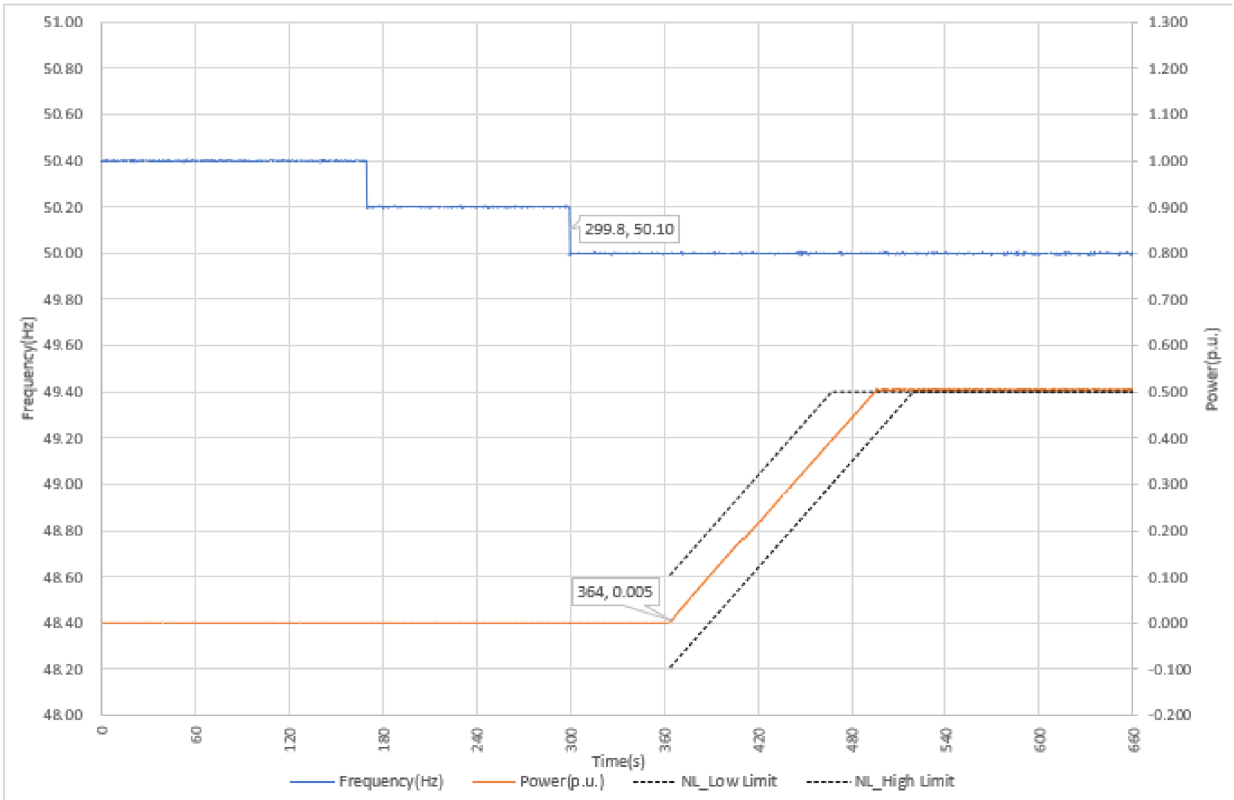
There is allowed a maximum tolerance for active power measurements up to ±5% of the staring power (P_M).

Test 1

PvsF behaviour

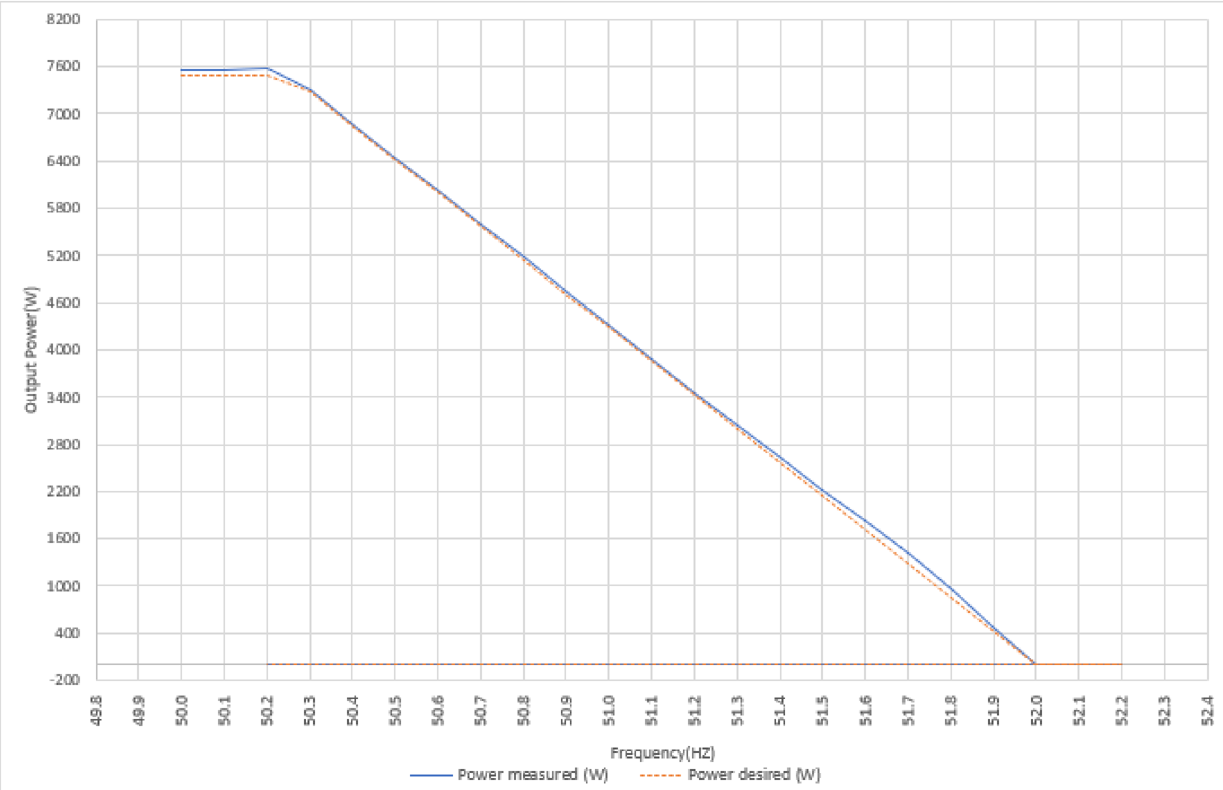


Reconnection Power gradient



Reconnection Value: 50.00 Hz	Reconnection time: 64.2 s
Increase of active power desired: 23.0 % Pn/min	Increase measured: 22.7 % Pn/min

Output power reduction



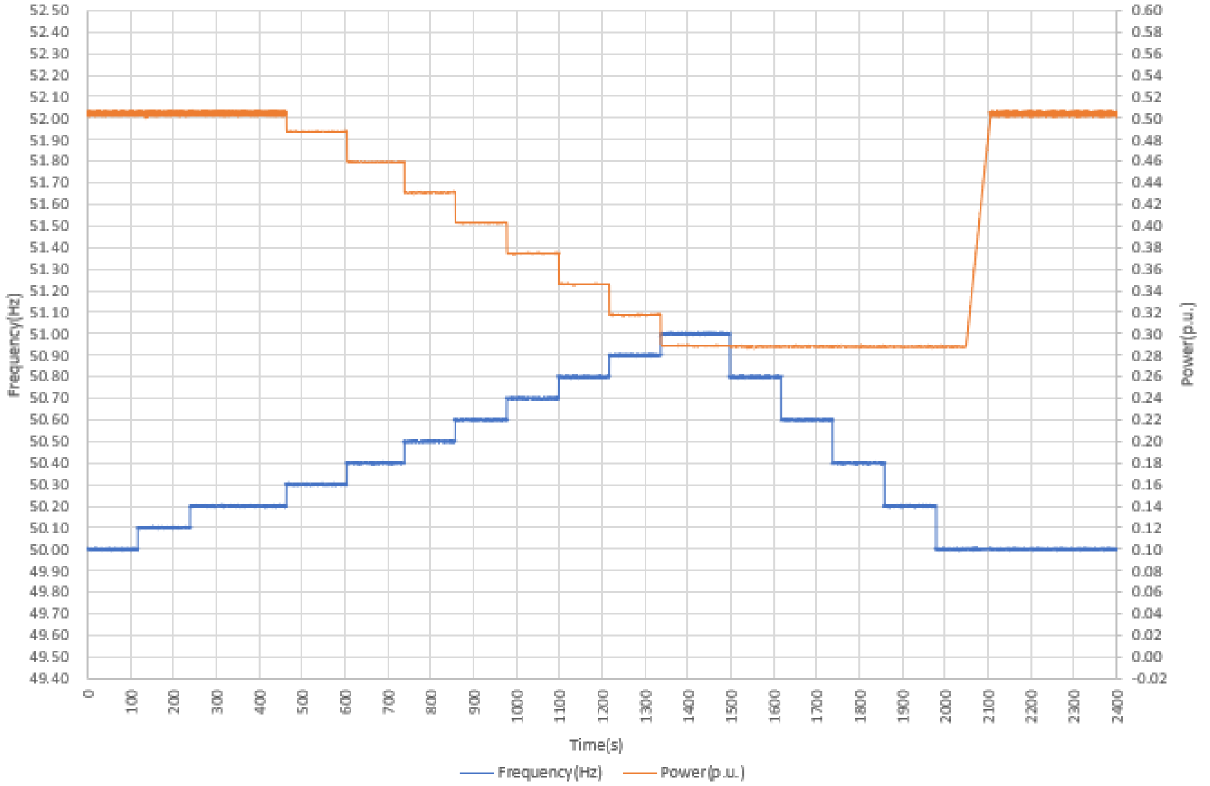
Test 2. Hysteresis capability and active power recovery				
%Pn	**Frequency (Hz)**	**Power measured (W)**	**Power desired (W)**	**ΔP (%P_M)**
50 %	50.00	7570	7500	0.93
	50.10	7569	7500	0.92
	50.20	7570	7500	0.93
	50.30	7315	7286	0.39
	50.40	6889	6857	0.42
	50.50	6463	6429	0.46
	50.60	6040	6000	0.53
	50.70	5615	5571	0.58
	50.80	5189	5143	0.62
	50.90	4760	4714	0.61
	51.00	4330	4286	0.59
	50.80	4320	4286	0.46
	50.60	4320	4286	0.46
	50.40	4319	4286	0.44
	50.20	4319	4286	0.44

There is allowed a maximum tolerance for active power measurements up to ±5% of the staring power (P_M).

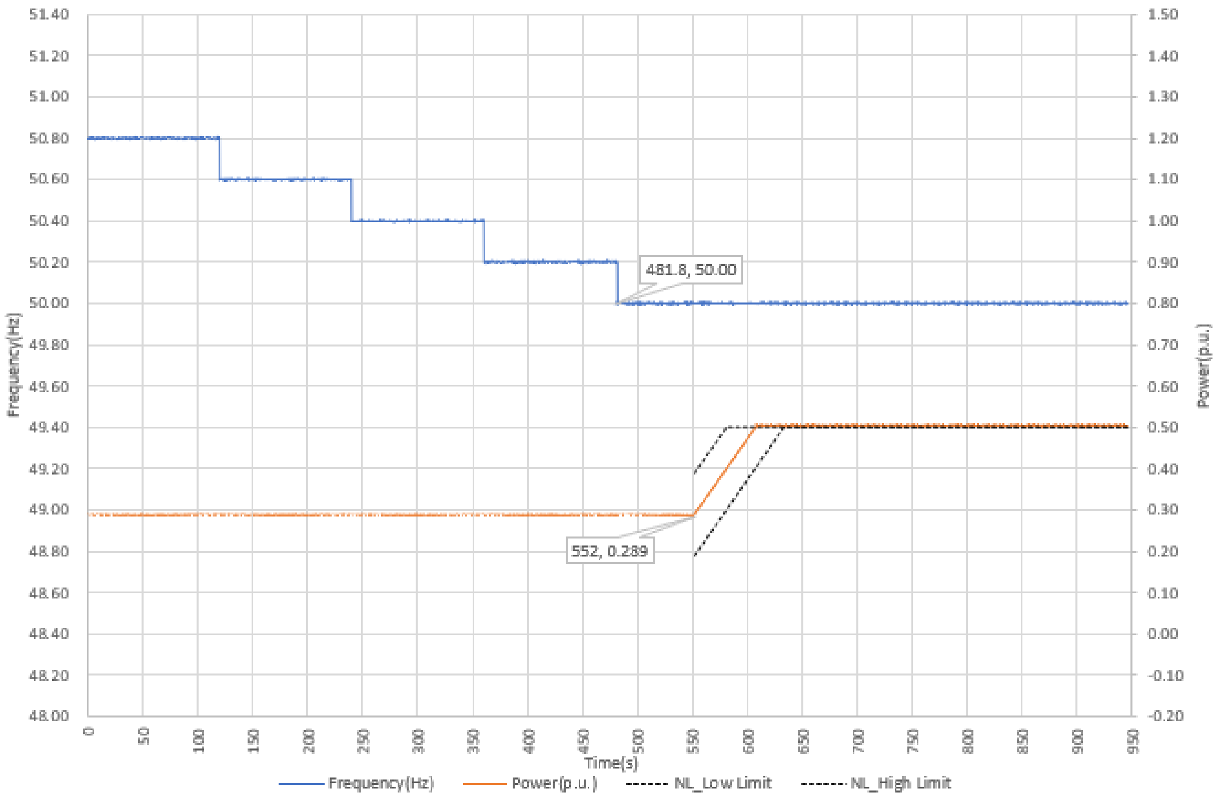
Test results are graphically shown in following pages.

Test 2

PvsF behaviour

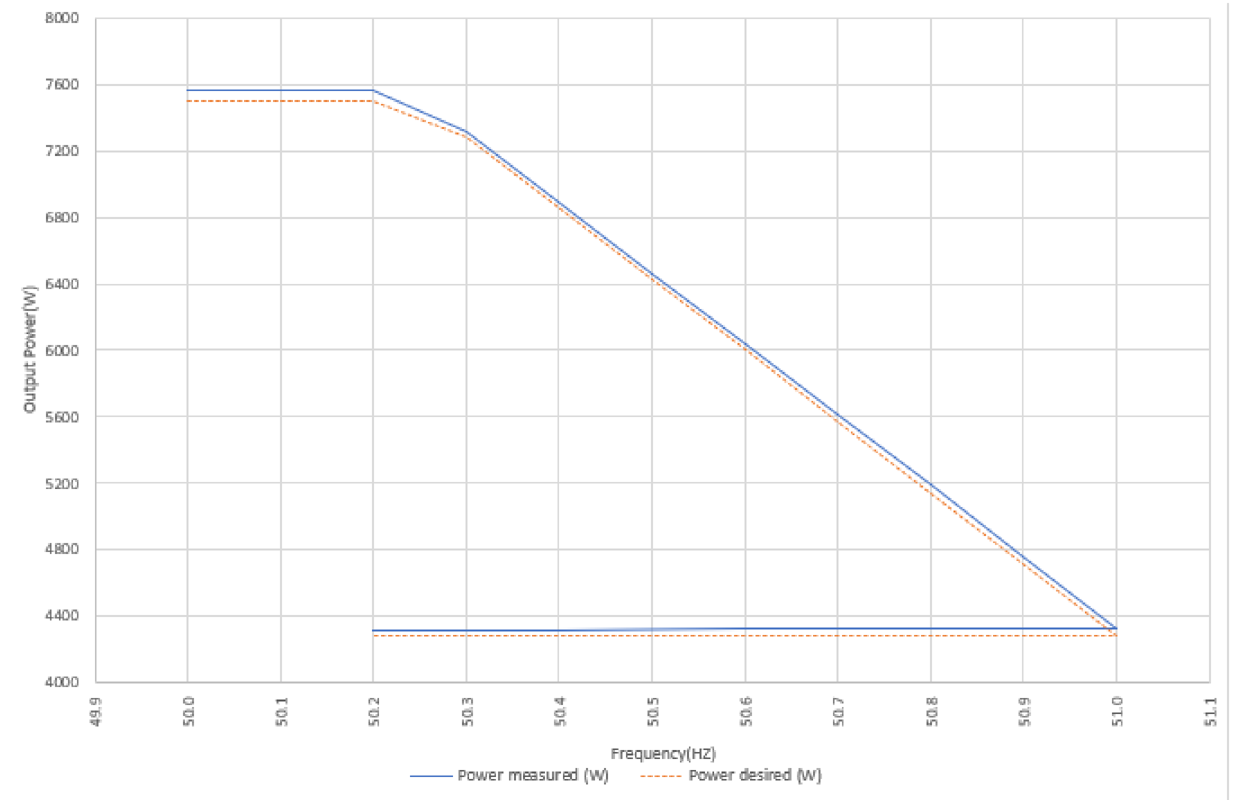


Power Recovery Gradient



Recovery Value: 50.00 Hz	Power recovery time: 70.2 s
Increase of active power desired: 23.0% Pn/min	Increase measured: 22.8% Pn/min

Output power reduction



4.20.2 Response to a decrease in grid frequency

This requirement applies only to inverters with energy storage. According to the clause 7.5.3.2, the inverter must be capable of supplying rated power between 49 Hz and 49.75 Hz for Australia.

- Test 1: Linear decrease of the active power up to disconnection in front of under frequency variations up to 49.0 Hz.
- Test 2: Hysteresis capability once over frequency variations are recovered up 49.85Hz.

When the inverter's frequency returns to operate with f >49.85 Hz, the active power must be recovered in both cases according to a power ramp limit and with a delay of at least 60 seconds.

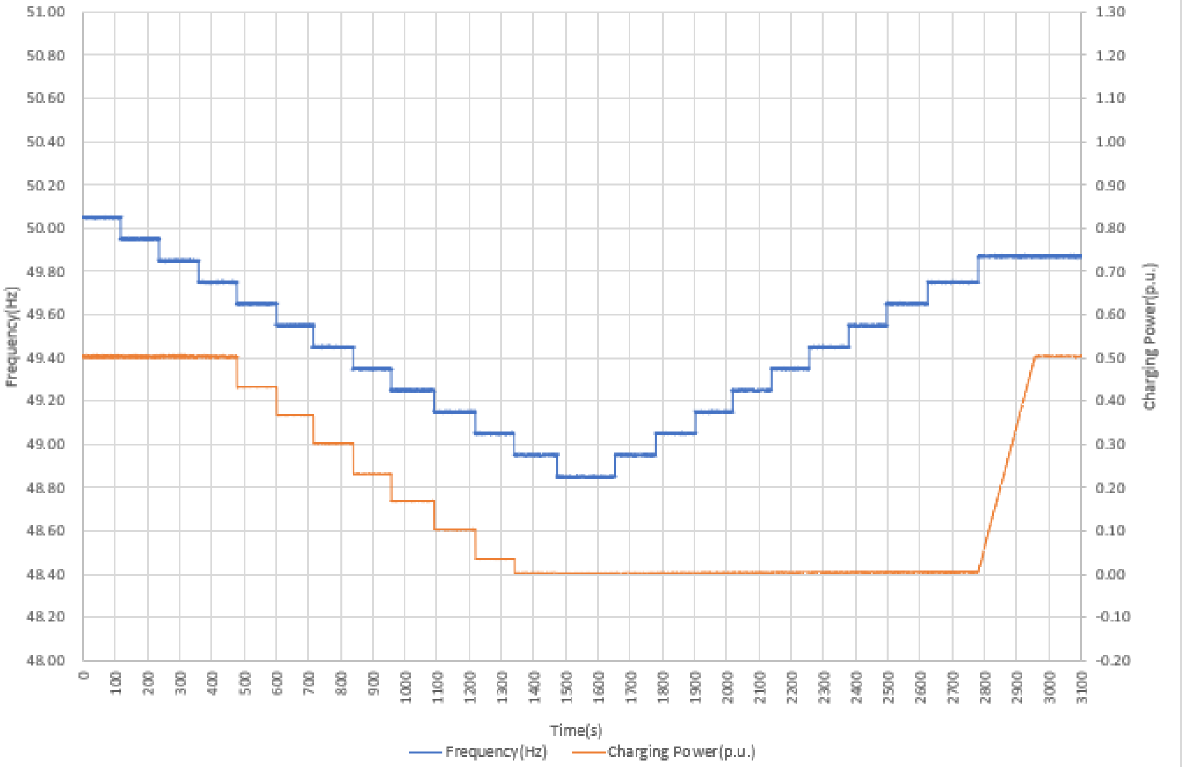
Test results obtained are shown in the following tables and graphs.

Test 1. Under frequency variations up to disconnection and active power recovery				
%Pn	**Frequency (Hz)**	**Charging Power measured (W)**	**Charging Power desired (W)**	**ΔP (%P_M)**
50 %	50.05	7547	7500	0.63
	49.95	7547	7500	0.63
	49.85	7540	7500	0.53
	49.75	7540	7500	0.54
	49.65	6494	6500	-0.08
	49.55	5517	5500	0.22
	49.45	4531	4500	0.41
	49.35	3469	3500	-0.41
	49.25	2526	2500	0.34
	49.15	1542	1500	0.55
	49.05	518	500	0.23
	48.95	38	0	0.50
	48.85	35	0	0.47
	48.95	37	0	0.50
	49.05	40	0	0.53
	49.15	43	0	0.57
	49.25	46	0	0.61
	49.35	49	0	0.65
	49.45	51	0	0.68
	49.55	54	0	0.72
	49.65	57	0	0.76
	49.75	60	0	0.79

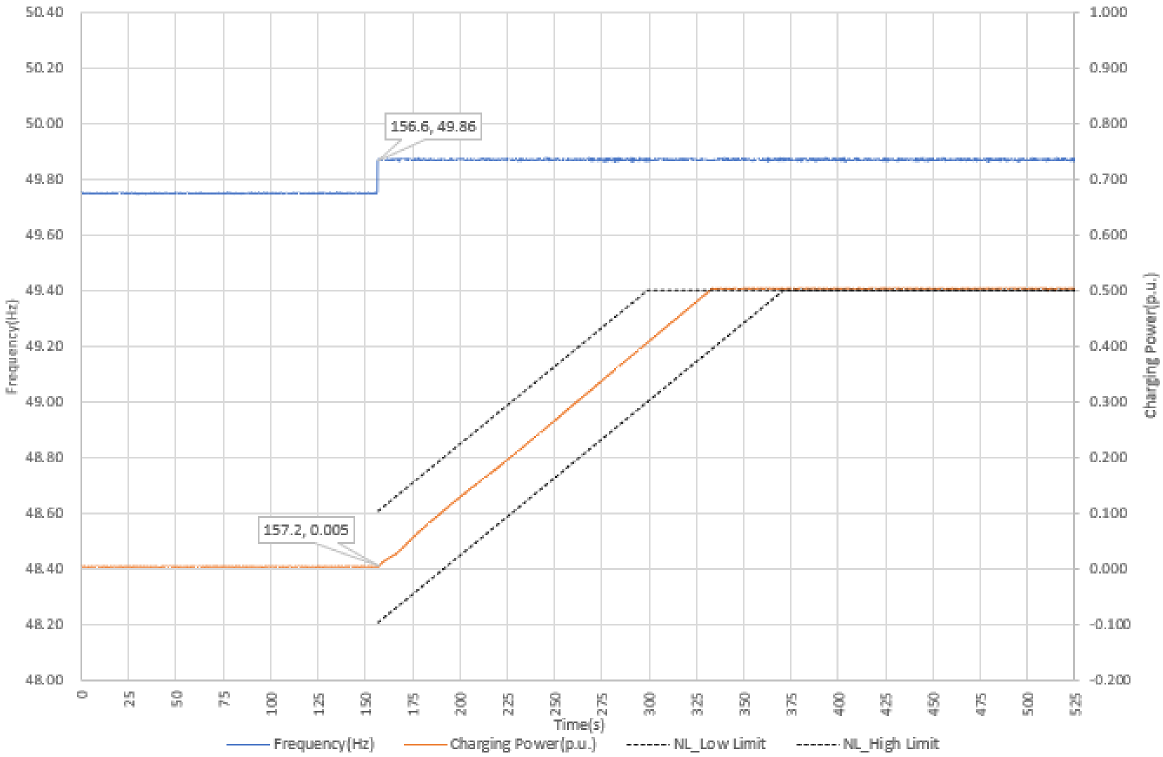
There is allowed a maximum tolerance for active power measurements up to ±5% of the staring power (P_M).

Test 1

PvsF behaviour

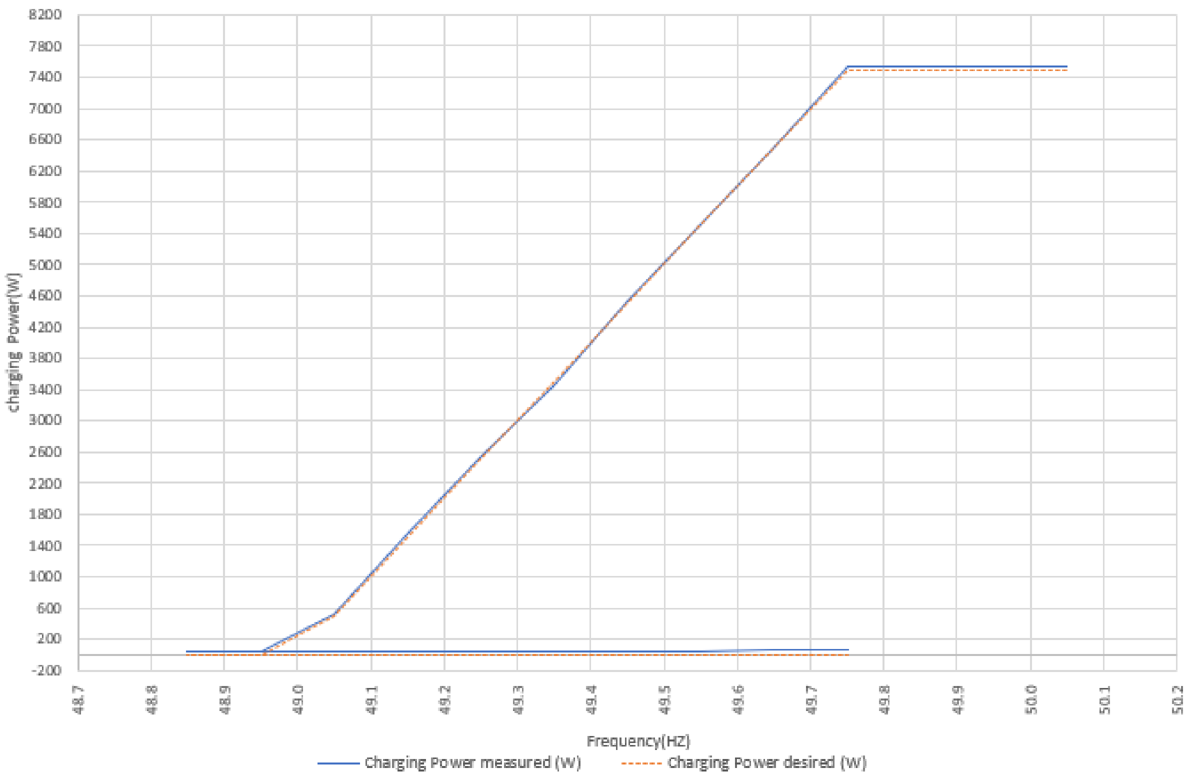


Reconnection Power gradient



Increase of active power desired: 16.7% Pn/min	Increase measured: 17.0 % Pn/min

Output power reduction



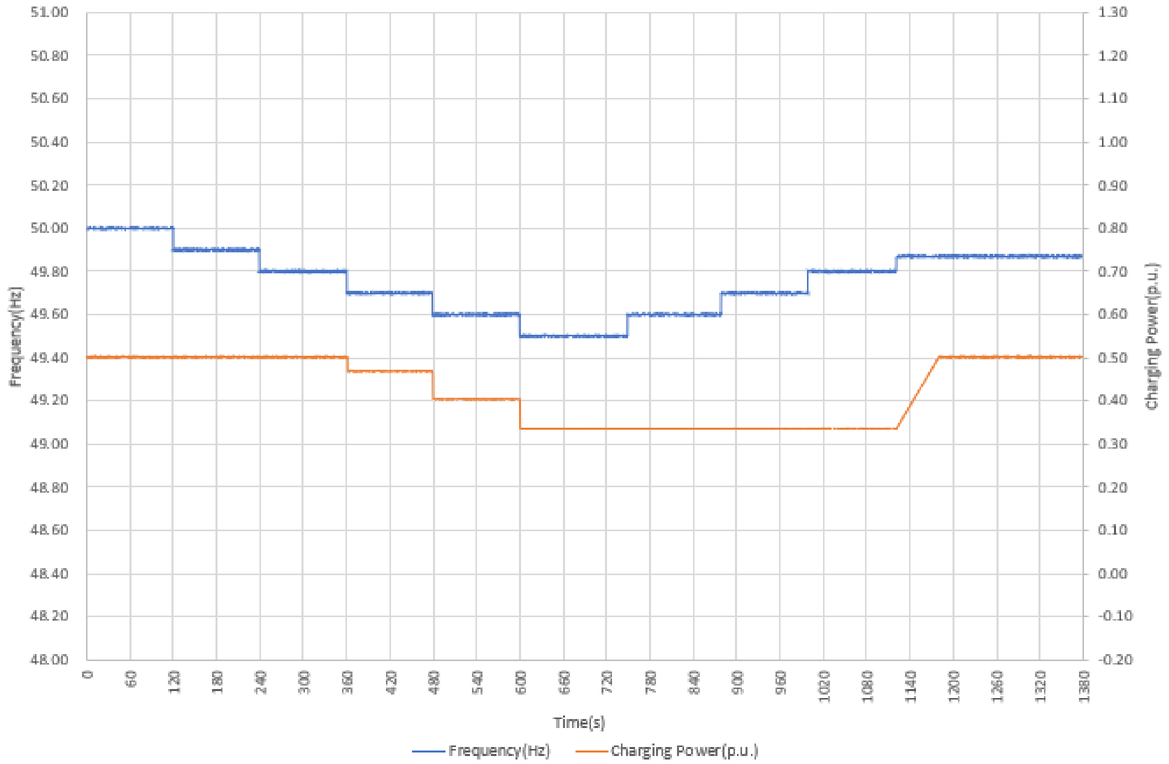
Test 2. Hysteresis capability and active power recovery				
%Pn	**Frequency (Hz)**	**Power measured (W)**	**Power desired (W)**	**ΔP (%P_M)**
50 %	50.00	7526	7500	0.35
	49.90	7526	7500	0.35
	49.80	7526	7500	0.35
	49.70	7025	7000	0.33
	49.60	6048	6000	0.64
	49.50	5035	5000	0.47
	49.60	5034	5000	0.45
	49.70	5037	5000	0.49
	49.80	5039	5000	0.51

There is allowed a maximum tolerance for active power measurements up to ±5% of the staring power (P_M).

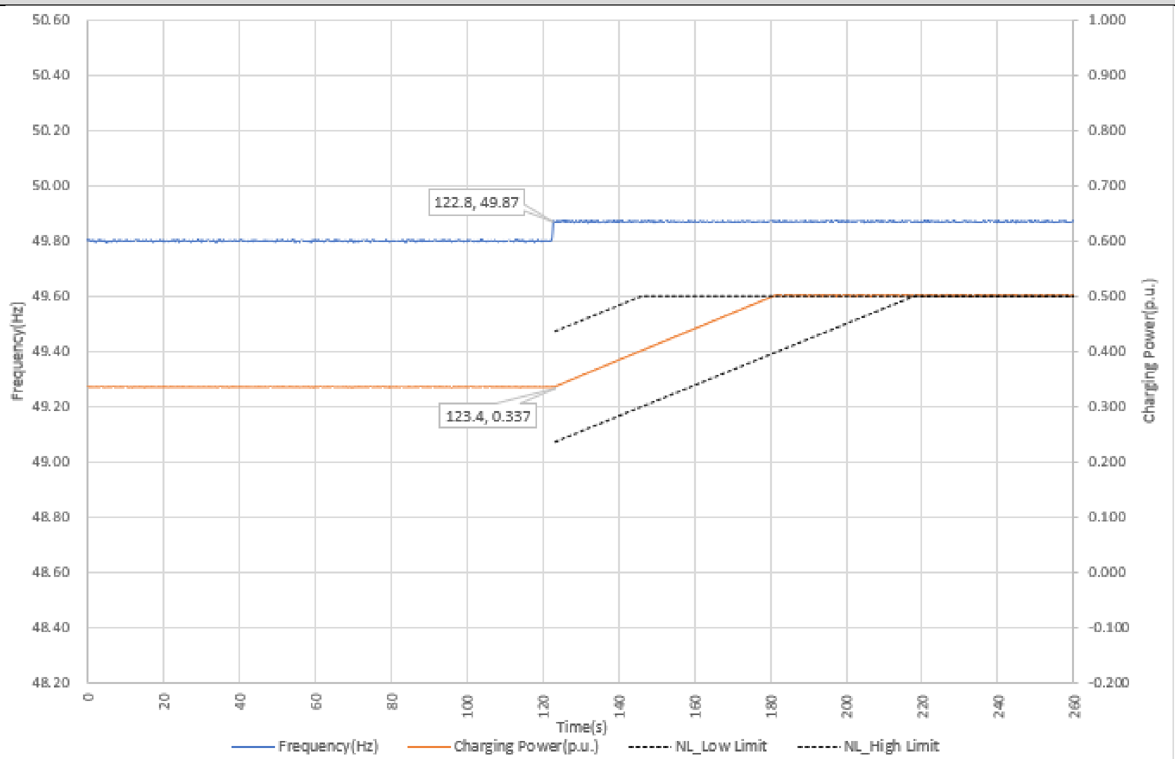
Test results are graphically shown in following pages.

Test 2

PvsF behaviour

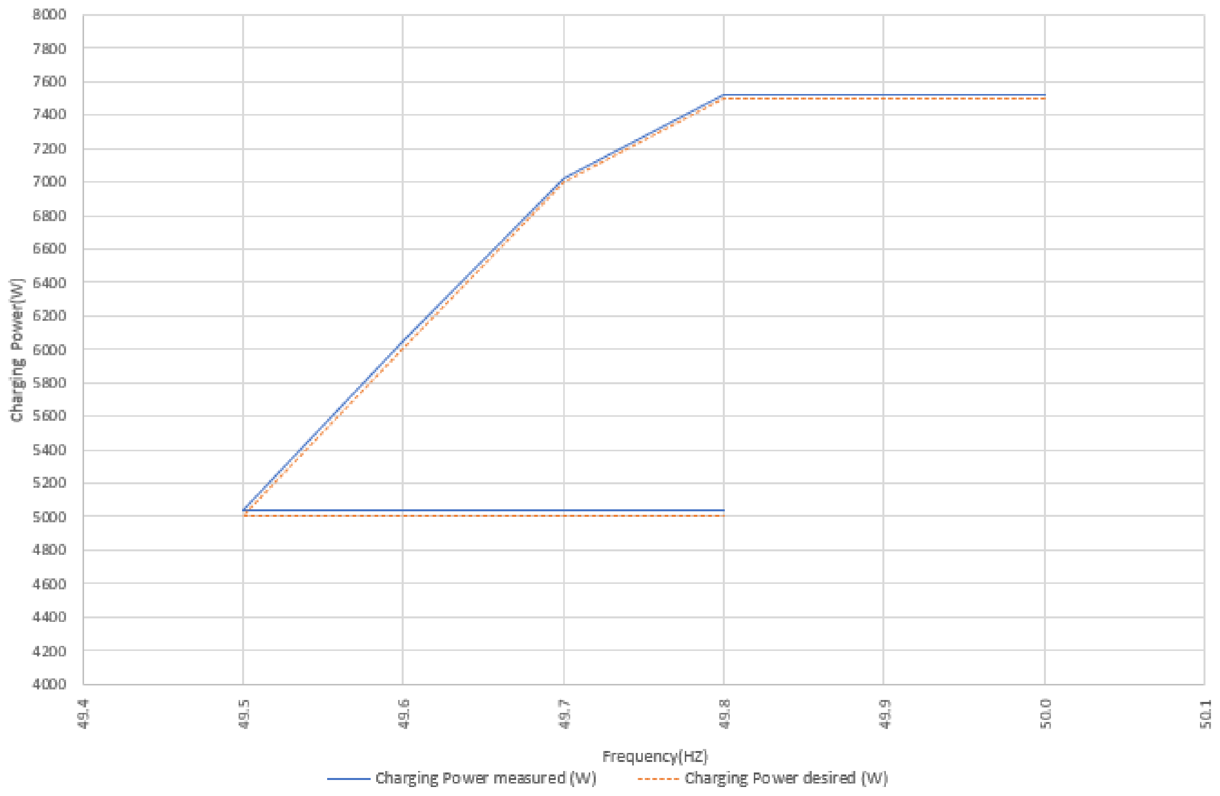


Reconnection and Power Gradient



Increase of active power desired: 16.7% Pn/min	Increase measured: 17.1% Pn/min

Output power reduction



4.21 DISCONNECTION ON EXTERNAL SIGNAL

The automatic disconnection device shall incorporate the ability to disconnect on an external signal.

If an external signal or demand response 'DRM 0' condition is asserted, the automatic disconnection device shall operate within 2 s.

Refer to point 4.12.1 for details.

4.22 CONNECTION AND RECONNECTION PROCEDURE

According to the clause 7.7 of the standard, voltage and frequency conditions for allowing the connection or reconnection of the equipment to the grid are as follows:

- The voltage of the grid has to be maintained within the limits of AS 60038, for Australia, for at least 60 s.
- The frequency of the grid has to be maintained within the range 47.5 Hz to 50.15 Hz for at least 60 s.

4.22.1 Frequency Connection

Test results are offered in the following tables:

Frequency Connection Value Limit (Hz)	No Connection Test			Connection Test		
	Frequency value (Hz)	Time measured (s)	Connection	Frequency value (Hz)	Connection	Time measured (s)
F ≥ 47.50	47.45	>120	☒ NO ☐ YES	47.55	☐ NO ☒ YES	64.8
F ≥ 47.50	47.45	>120	☒ NO ☐ YES	47.55	☐ NO ☒ YES	65.2
F ≥ 47.50	47.45	>120	☒ NO ☐ YES	47.55	☐ NO ☒ YES	65.6
F ≤ 50.15	50.20	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	63.6
F ≤ 50.15	50.20	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	65.8
F ≤ 50.15	50.20	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	65.6

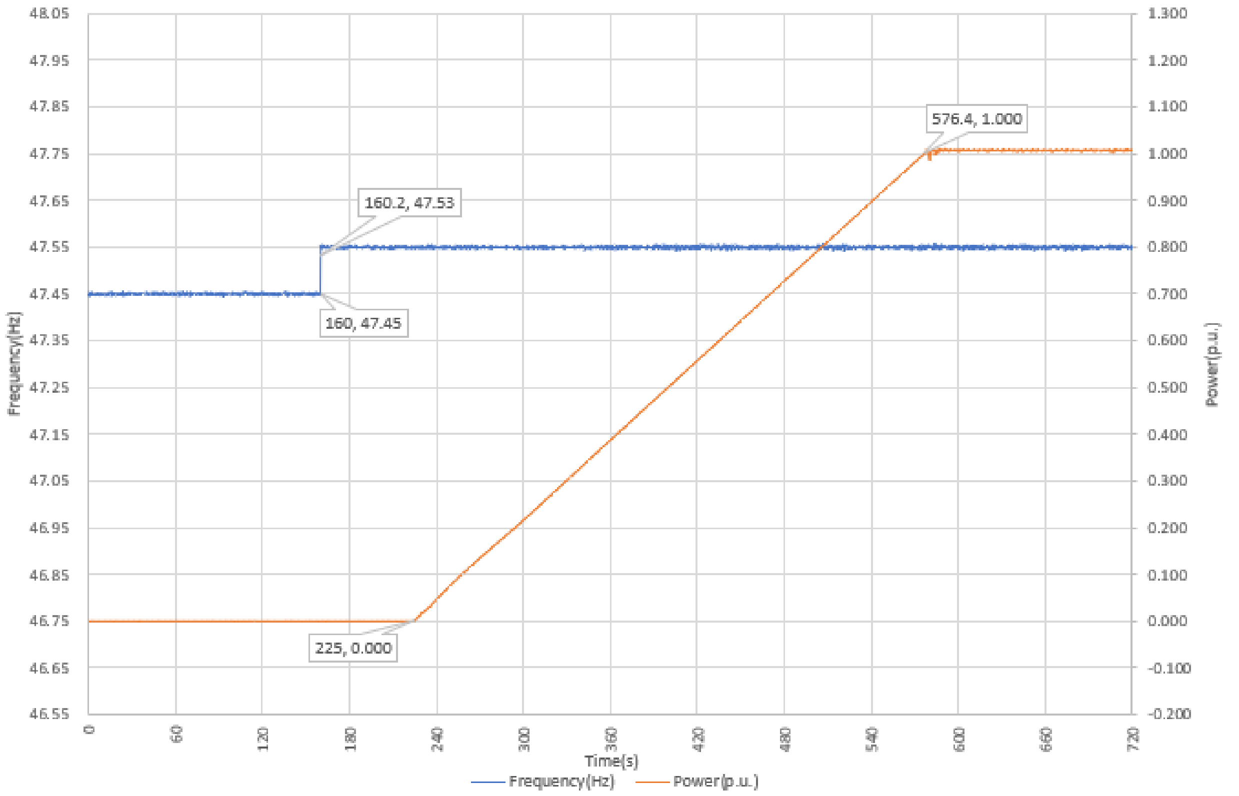
In addition to this requirement, it has been verified that according to the point 7.7 of the standard, the Control System of the inverter has a function to start connection following an adjustable Ramp Rate. In this case, the adjusted gradient has been an increasing rate of 16.7%Pn per minute.

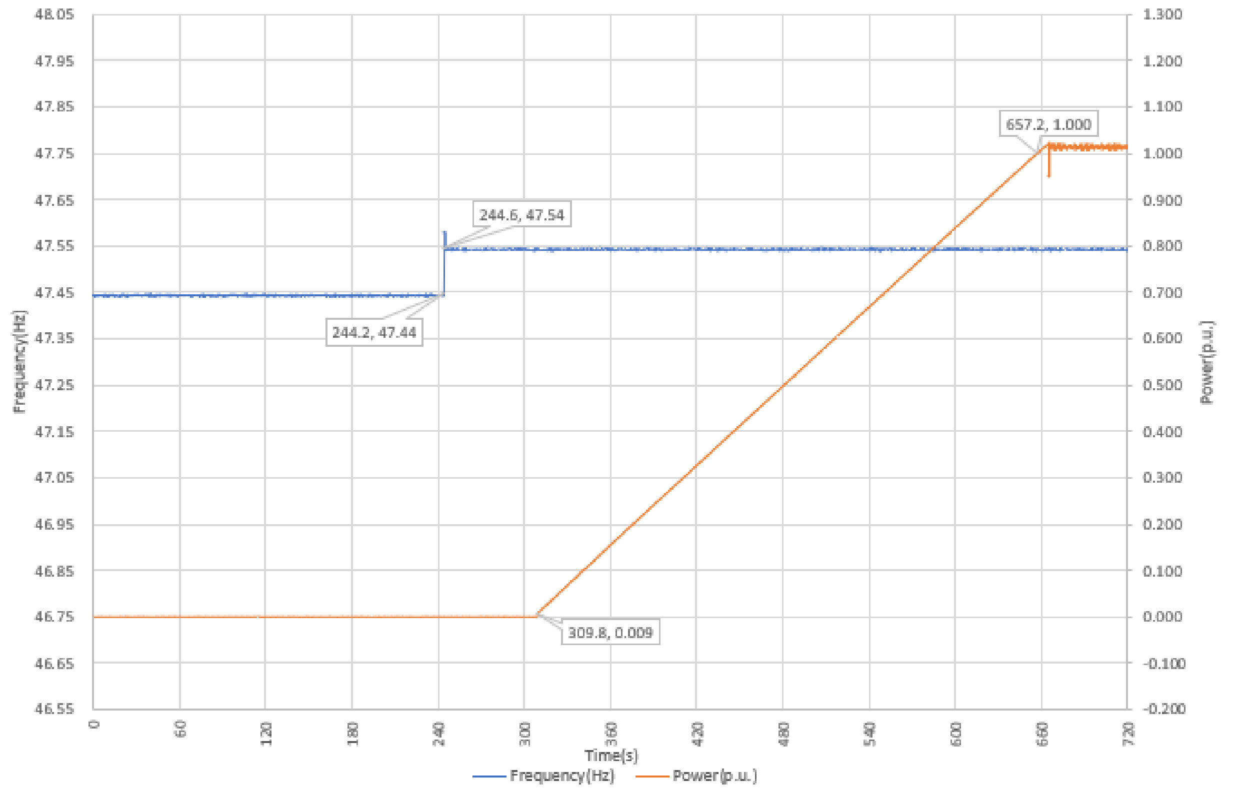
Frequency Connection Value Limit	Gradient (ΔP) desired (%Pn/min)	Gradient measured (%P_n/min)
F ≥ 47.50 Hz	16.7	17.1/17.3/17.3
F ≤ 50.15 Hz	16.7	17.0/17.3/17.3

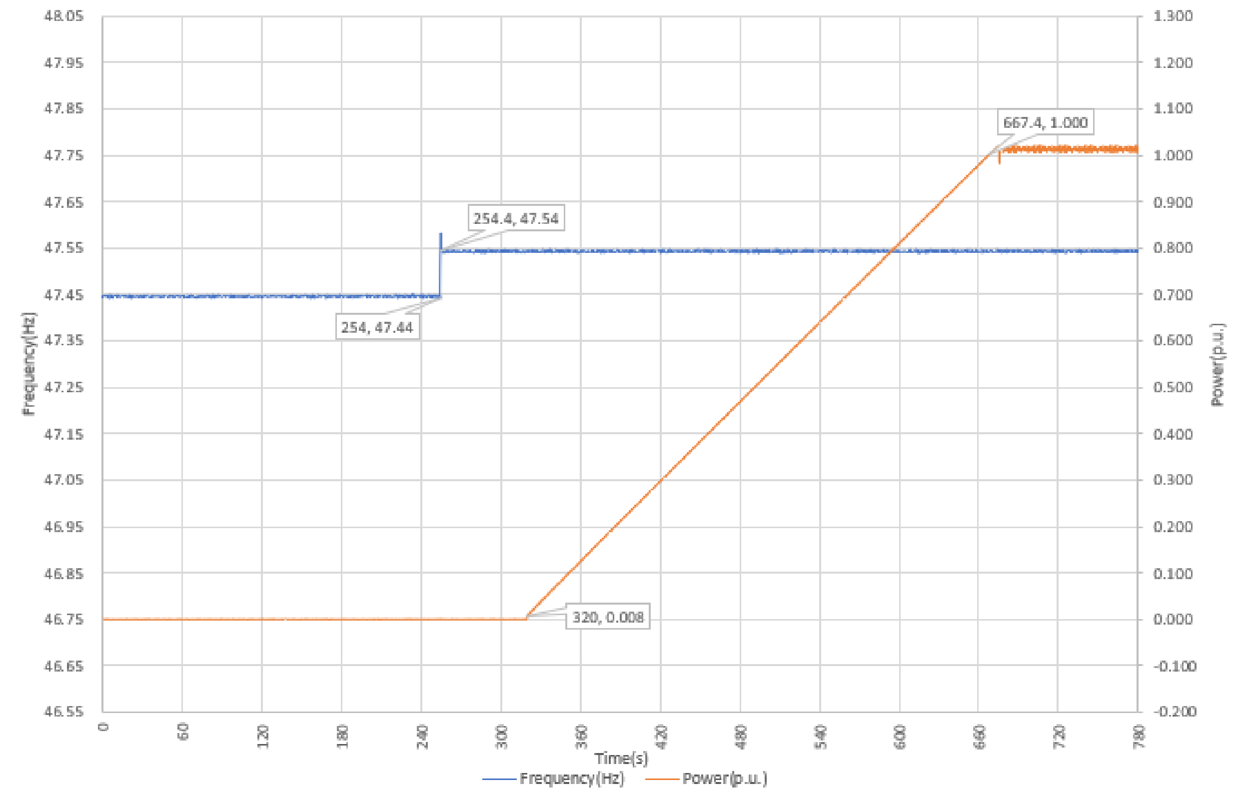
Note: it has been considered a minimum delay of 60 seconds to proceed with the start-up once the equipment is inside the required ranges.

Test results are graphically shown in following pages.

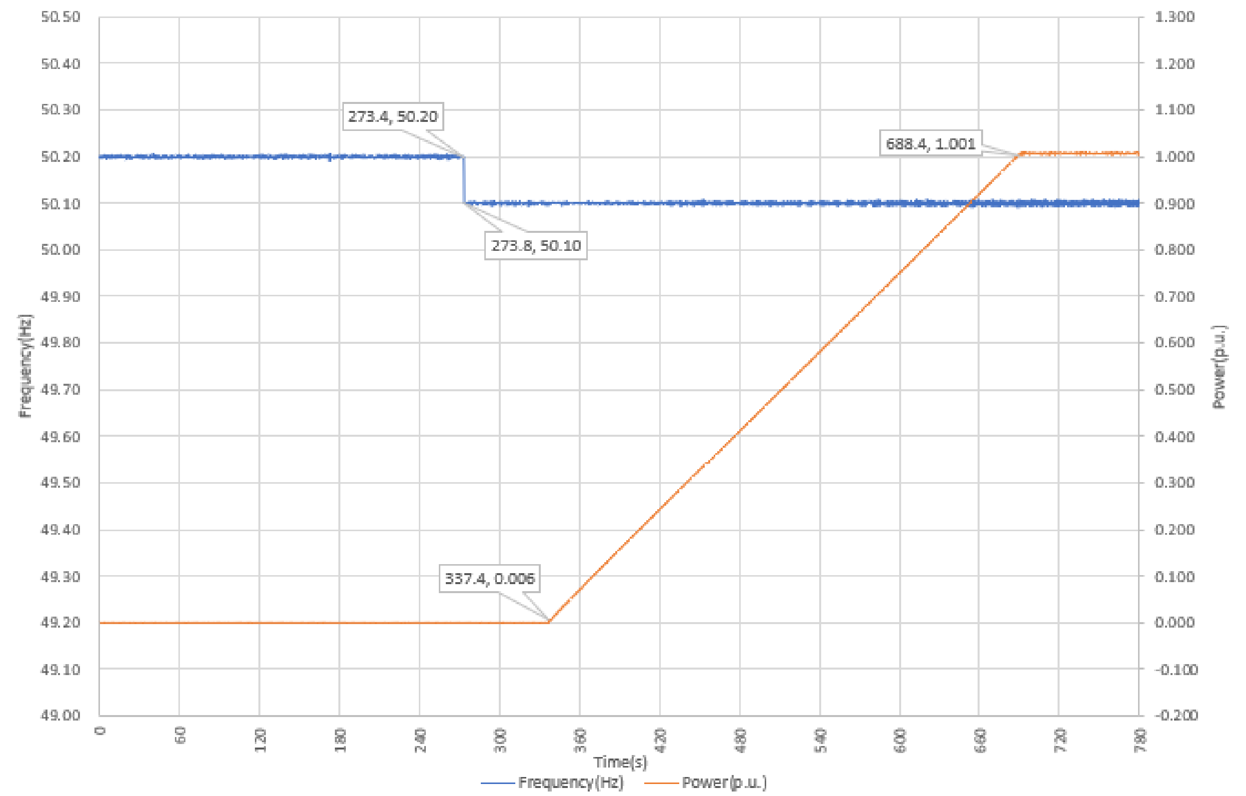
Under Frequency Connection

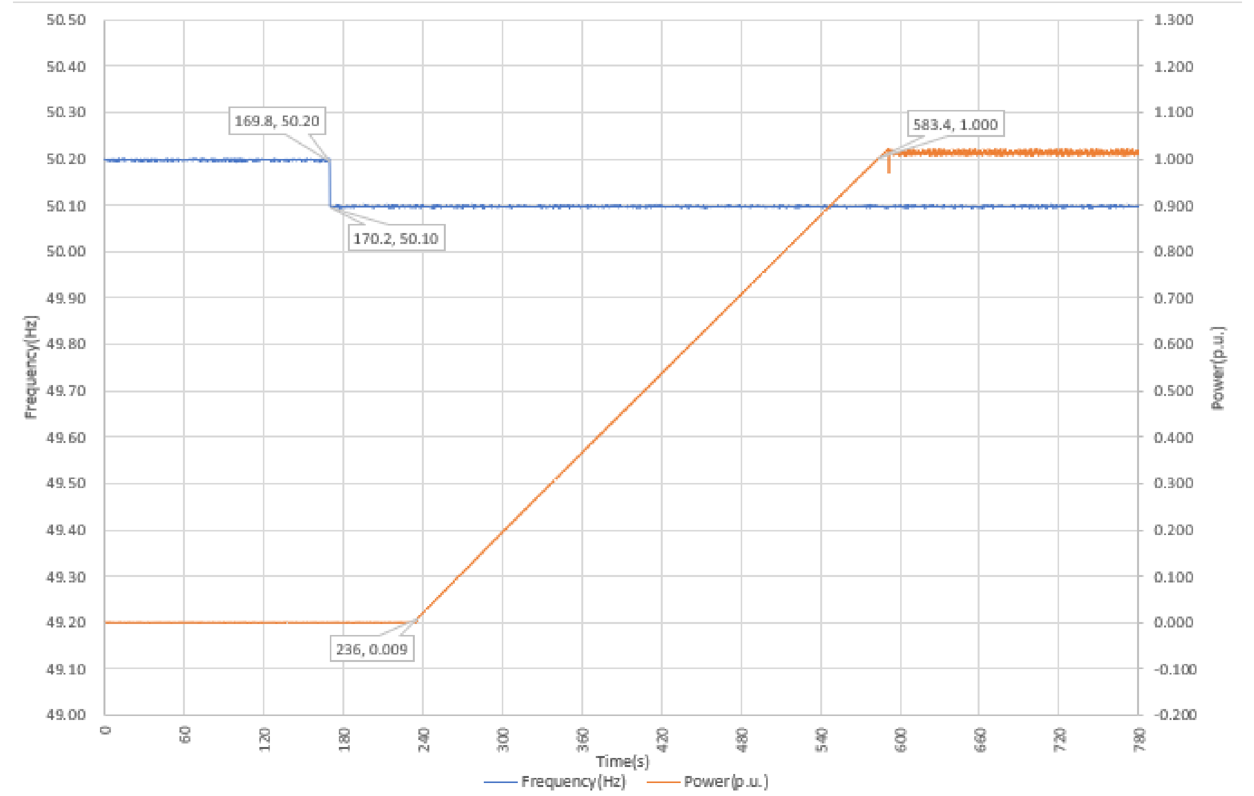


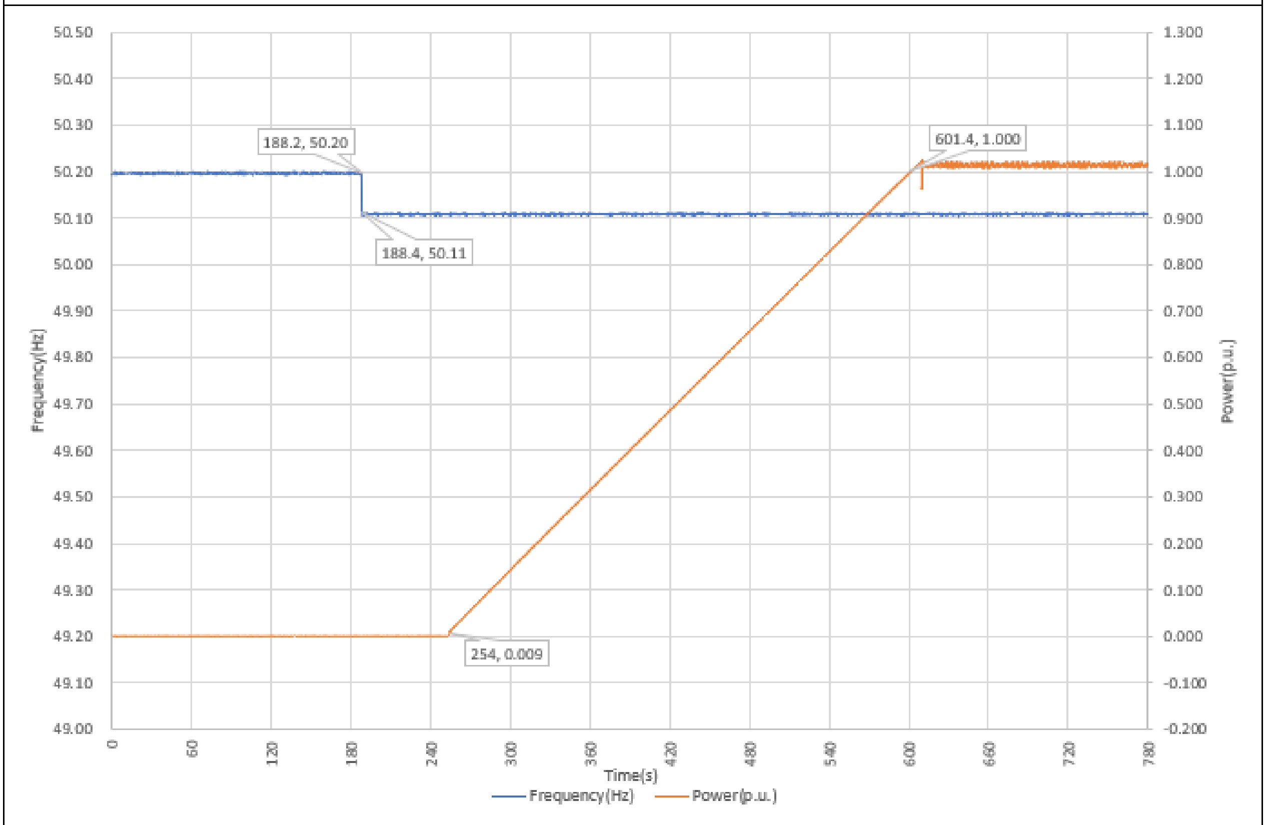




Over Frequency Connection




169.8, 50.20
170.2, 50.10
583.4, 1.000
236, 0.009
Frequency(Hz)
Power(p.u.)
Time(s)


188.2, 50.20
188.4, 50.11
601.4, 1.000
254, 0.009
Frequency(Hz)
Power(p.u.)
Time(s)

4.22.2 Frequency Reconnection

Test results are offered in the following tables:

Frequency Reconnection Value Limit	No Reconnection Test			Reconnection Test		
	Frequency value (Hz)	Time measured (s)	Reconnection	Frequency value (Hz)	Reconnection	Time measured (s)
F ≥ 47.50 Hz	47.40	>120	☒ NO ☐ YES	47.60	☐ NO ☒ YES	72.8
F ≥ 47.50 Hz	47.40	>120	☒ NO ☐ YES	47.60	☐ NO ☒ YES	64.0
F ≥ 47.50 Hz	47.40	>120	☒ NO ☐ YES	47.60	☐ NO ☒ YES	63.8
F ≤ 50.15 Hz	50.25	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	64.0
F ≤ 50.15 Hz	50.25	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	63.8
F ≤ 50.15 Hz	50.25	>120	☒ NO ☐ YES	50.10	☐ NO ☒ YES	64.0

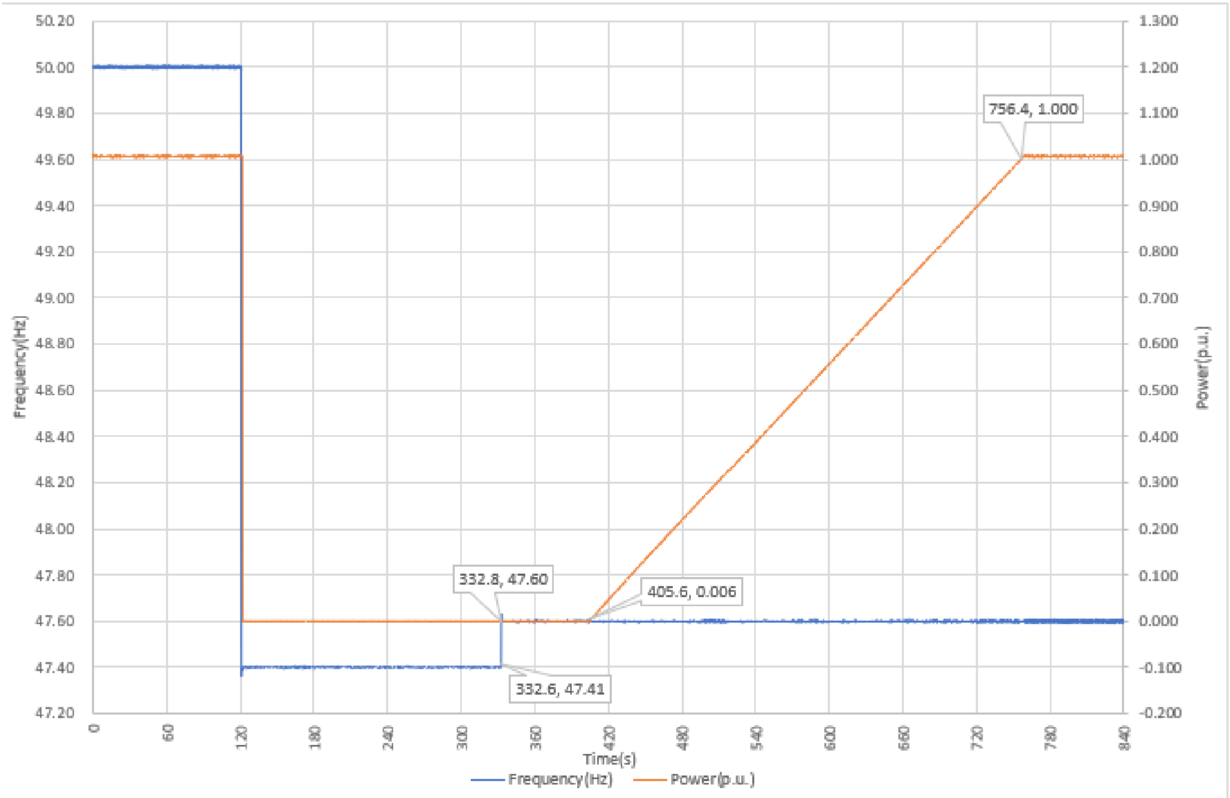
In addition to this requirement, it has been verified that according to the point 7.7 of the standard, the Control System of the inverter has a function to start reconnection following an adjustable Ramp Rate. In this case, the adjusted gradient has been an increasing rate of 16.7%Pn per minute.

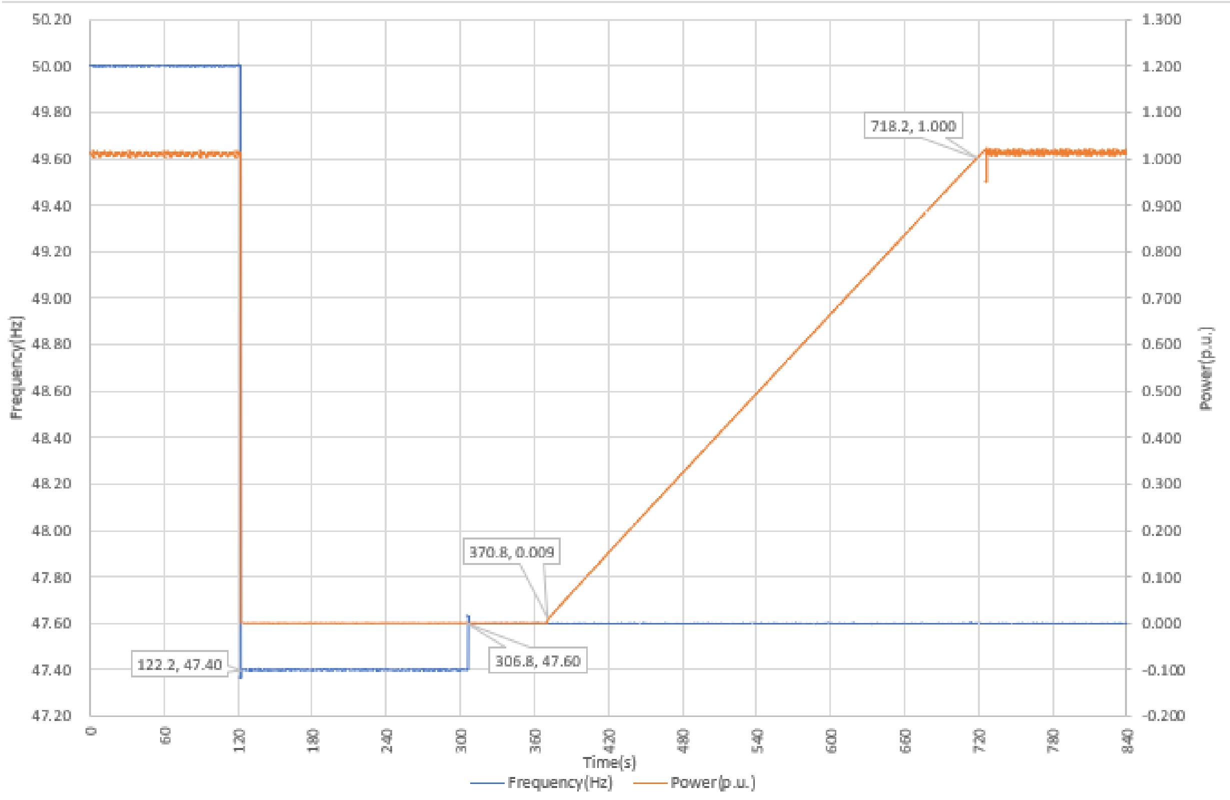
Frequency Reconnection Value Limit	Gradient (ΔP) desired (%P_n/min)	Gradient measured (%P_n/min)
F ≥ 47.50 Hz	16.7	17.0/17.3/17.3
F ≤ 50.15 Hz	16.7	17.0/17.3/17.3

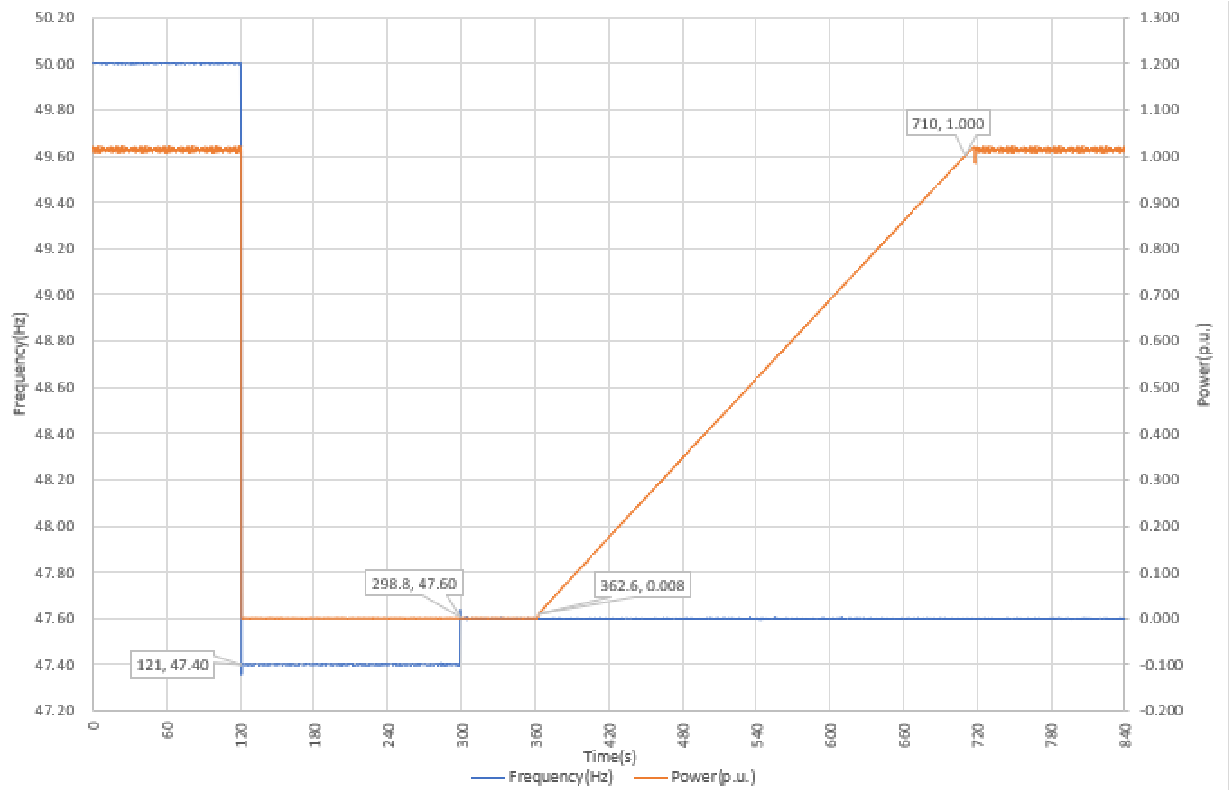
Note: it has been considered a minimum delay of 60 seconds to proceed with the start-up once the equipment is inside the required ranges.

Test results are graphically shown in following pages.

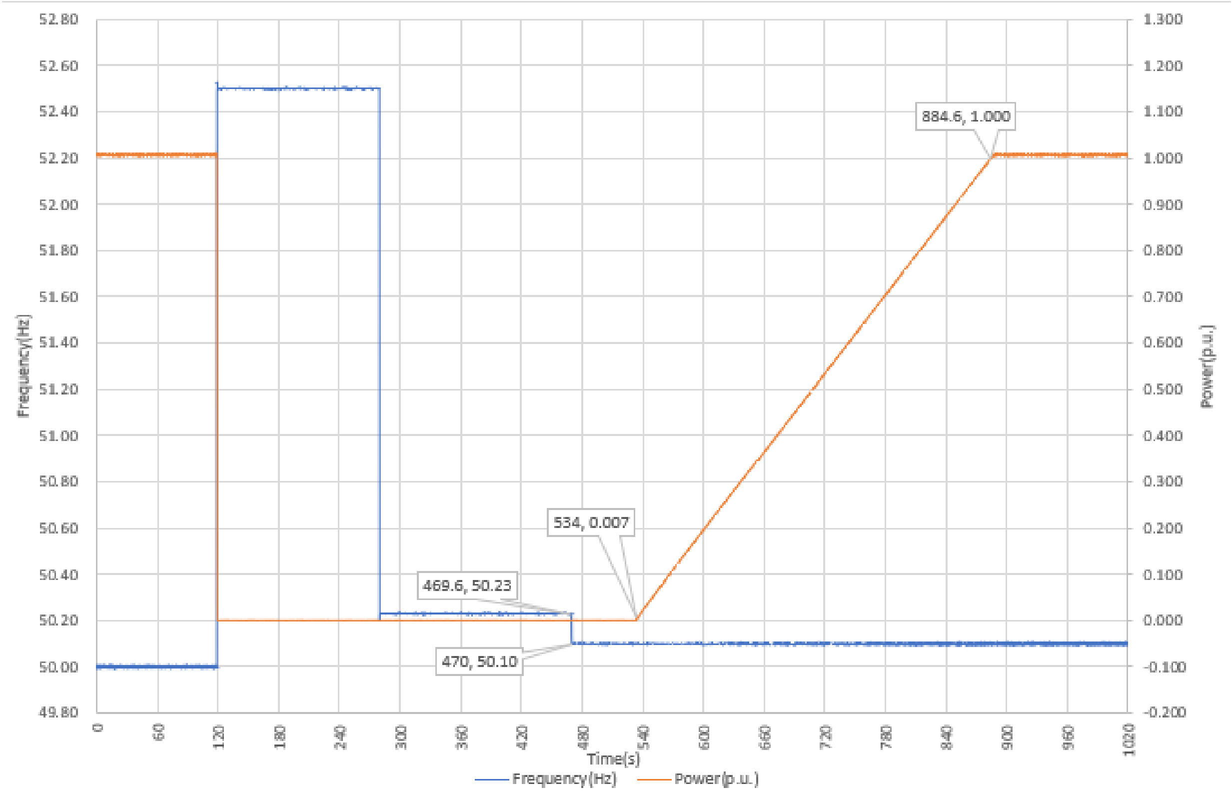
Under Frequency Reconnection

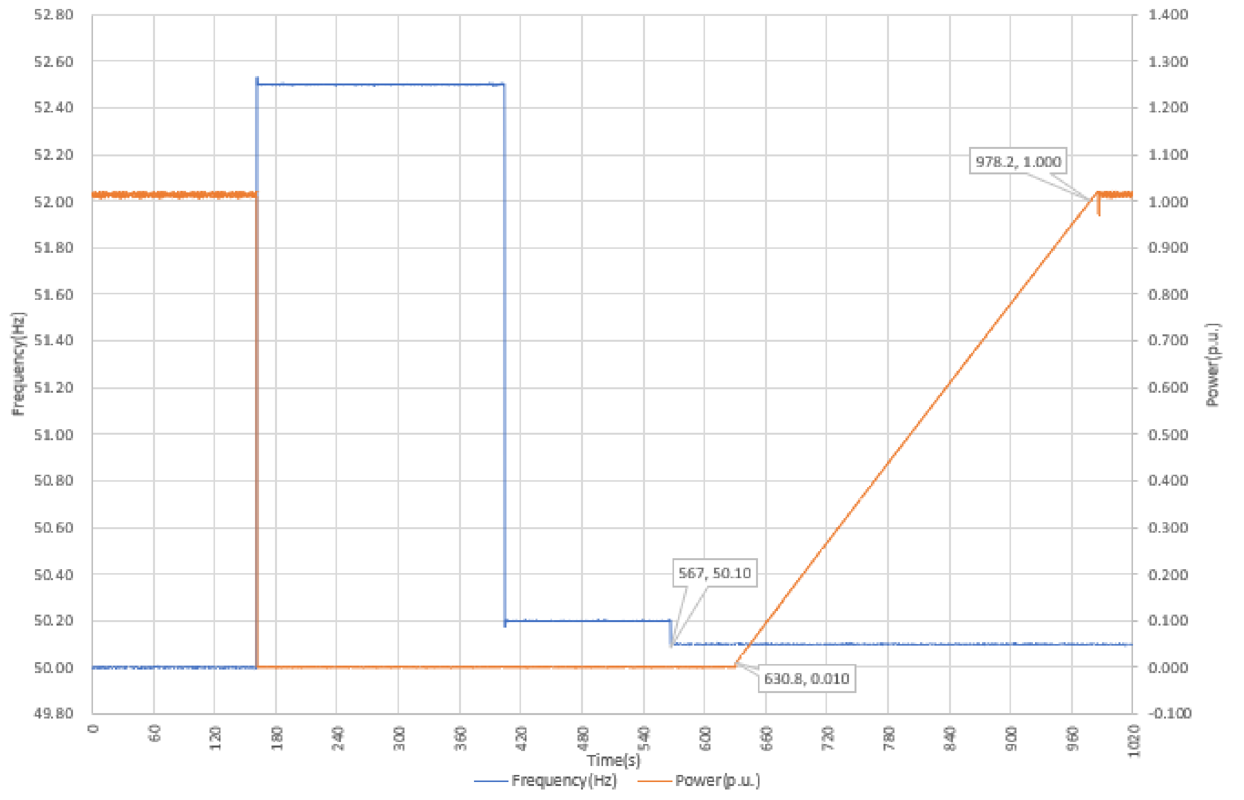


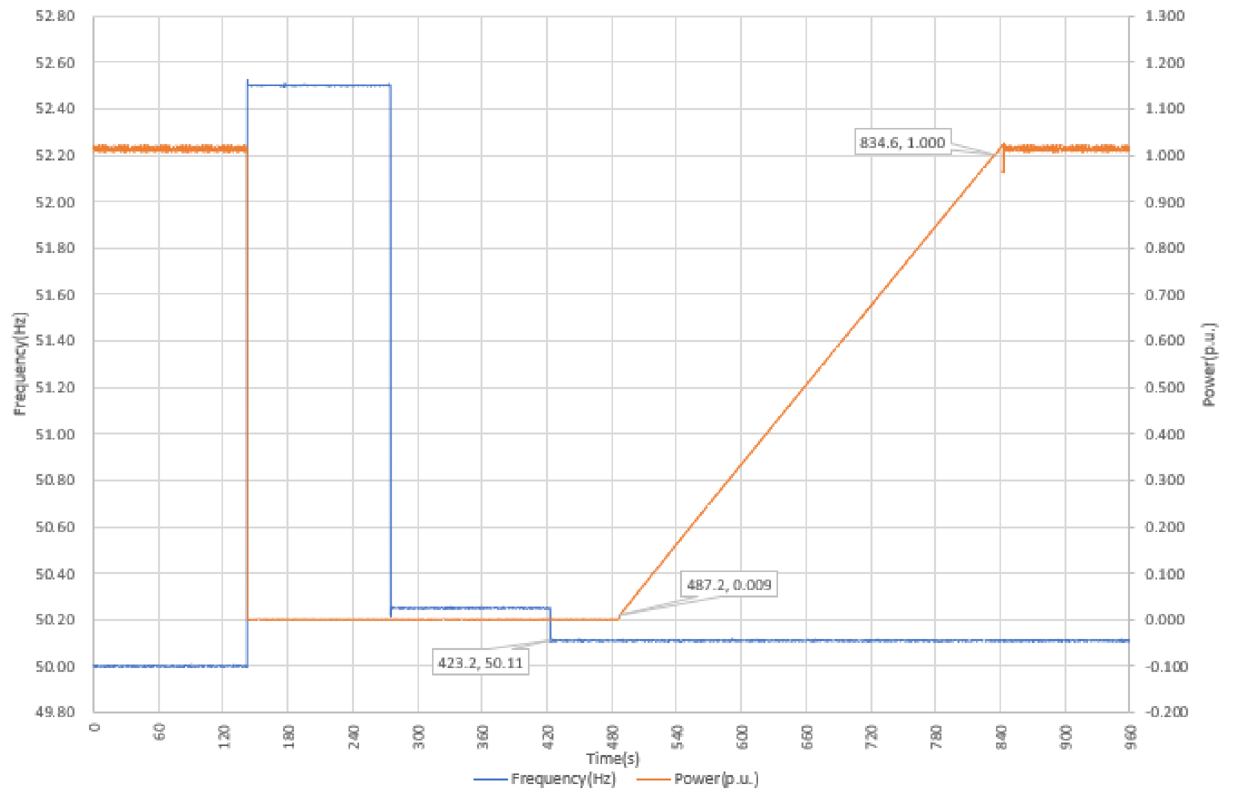




Over Frequency Reconnection




978.2, 1.000
567, 50.10
630.8, 0.010
Frequency(Hz)
Power(p.u.)
Time(s)


834.6, 1.000
487.2, 0.009
423.2, 50.11
Frequency(Hz)
Power(p.u.)
Time(s)

4.22.3 Voltage Connection

Test results are offered in the following tables:

Voltage Connection Value Limit	No Connection Test			Connection Test		
	Voltage value (%Un)	Time measured (s)	Connection	Voltage value (%Un)	Connection	Time measured (s)
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	64.2
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	66.6
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	65.6
V ≤ 110.0% Un	110.5%	>120	☒ NO ☐ YES	109.4%	☐ NO ☒ YES	63.8
V ≤ 110.0% Un	110.5%	>120	☒ NO ☐ YES	109.4%	☐ NO ☒ YES	65.2
V ≤ 110.0% Un	110.5%	>120	☒ NO ☐ YES	109.4%	☐ NO ☒ YES	65.0

The standard states that the tolerance limit for voltage connection values is ± 2 V, which is a 0,8% Un over 230 V, the reference voltage considered by the standard. So, 0.8% Un is the allowed tolerance to be considered for voltage connection value tests.

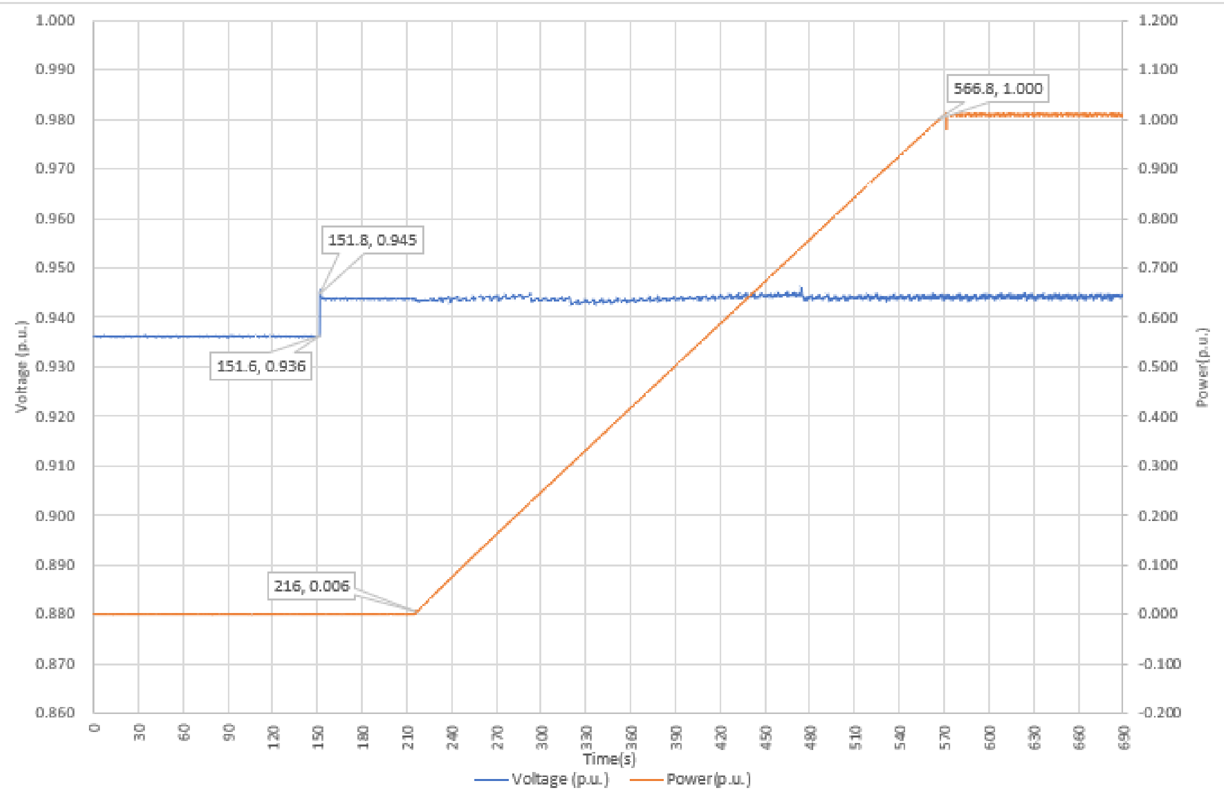
In addition to this requirement, it has been verified that according to the point 7.7 of the standard, the Control System of the inverter has a function to start connection following an adjustable Ramp Rate. The following table shows the programmed gradient for the different reconnections:

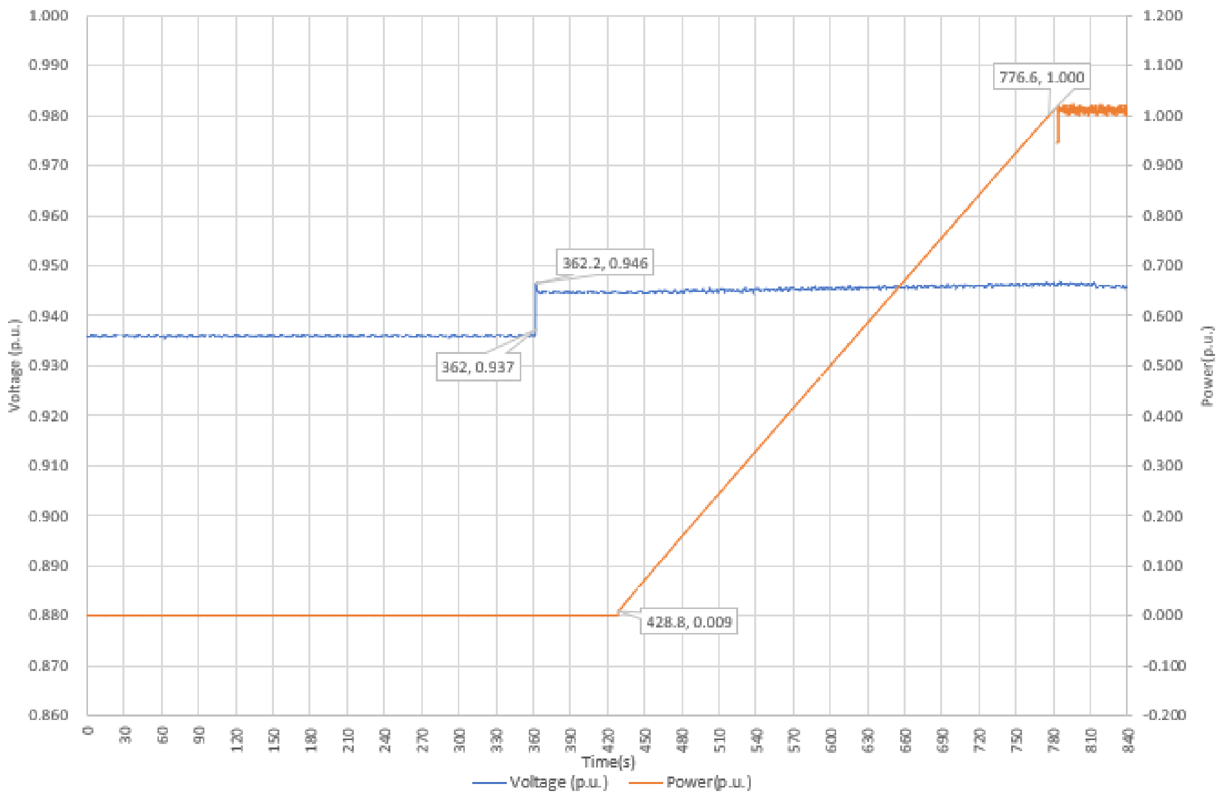
Voltage Connection Value Limit	Gradient (ΔP) desired ($\%P_n$/min)	Gradient measured ($\%P_n$/min)
V ≥ 94.0% Un	16.7	17.0/17.3/17.3
V ≤ 110.0% Un	16.7	17.0/17.3/17.3

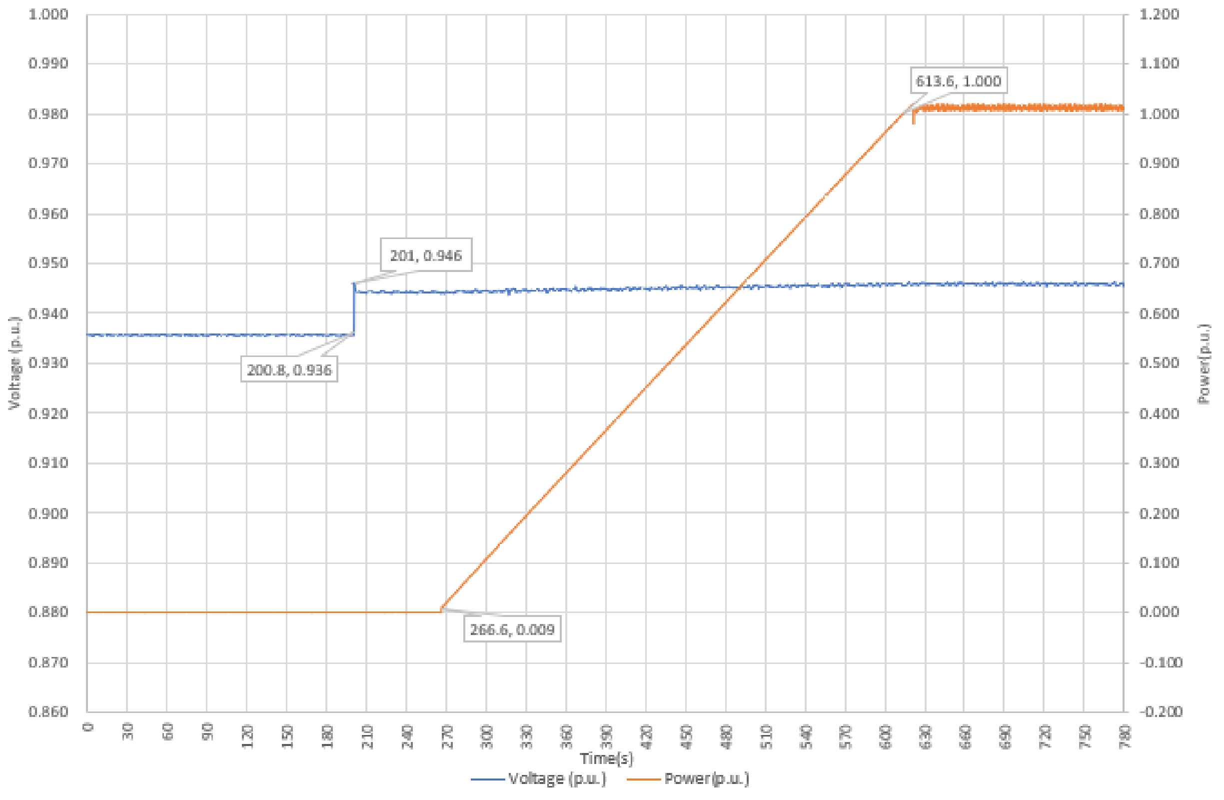
Note: it has been considered a minimum delay of 60 seconds to proceed with the start-up once the equipment is inside the required ranges.

Test results are graphically shown in following pages.

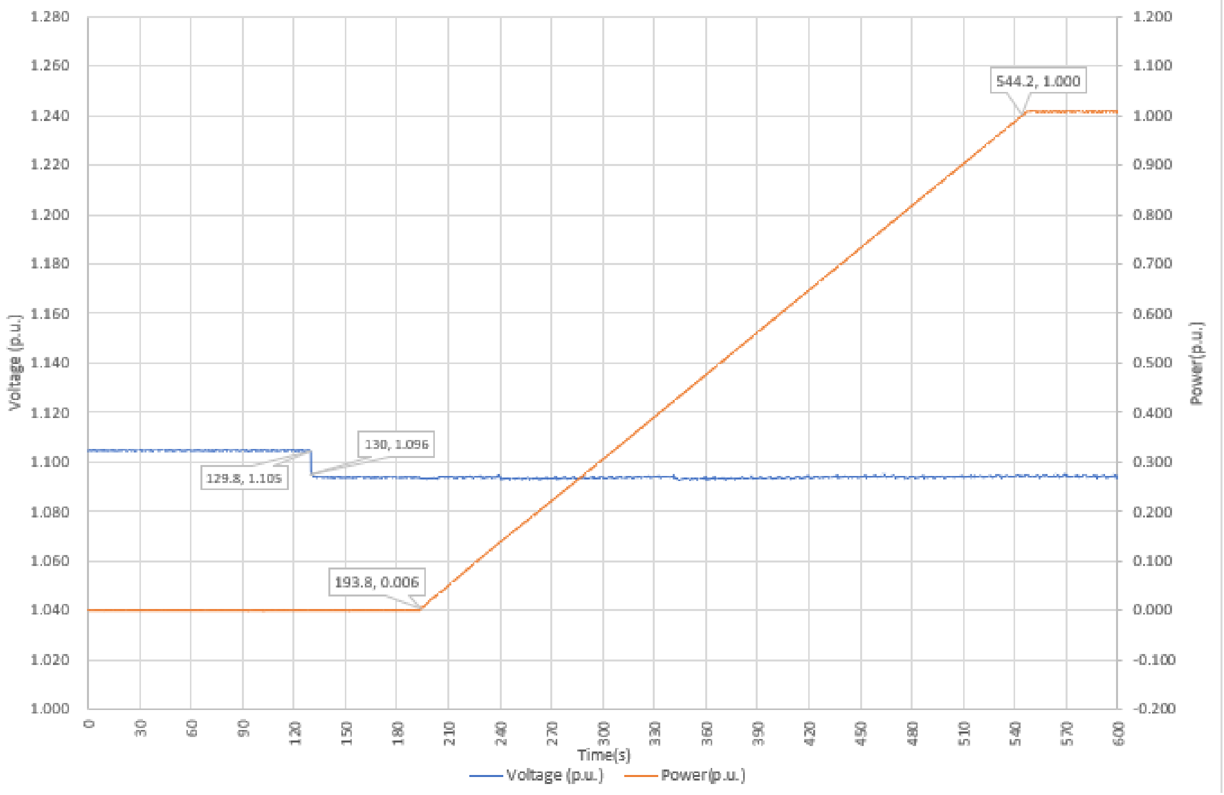
Under Voltage Connection

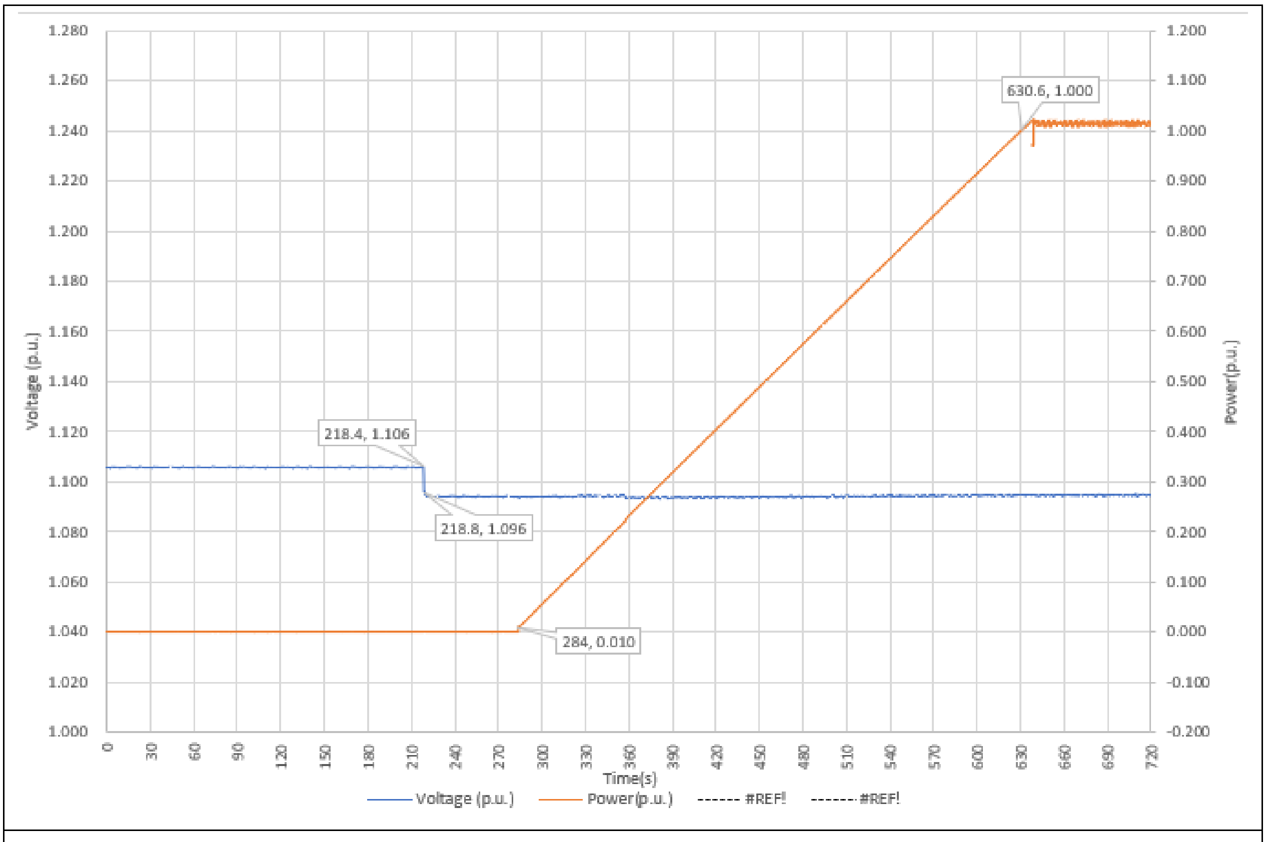




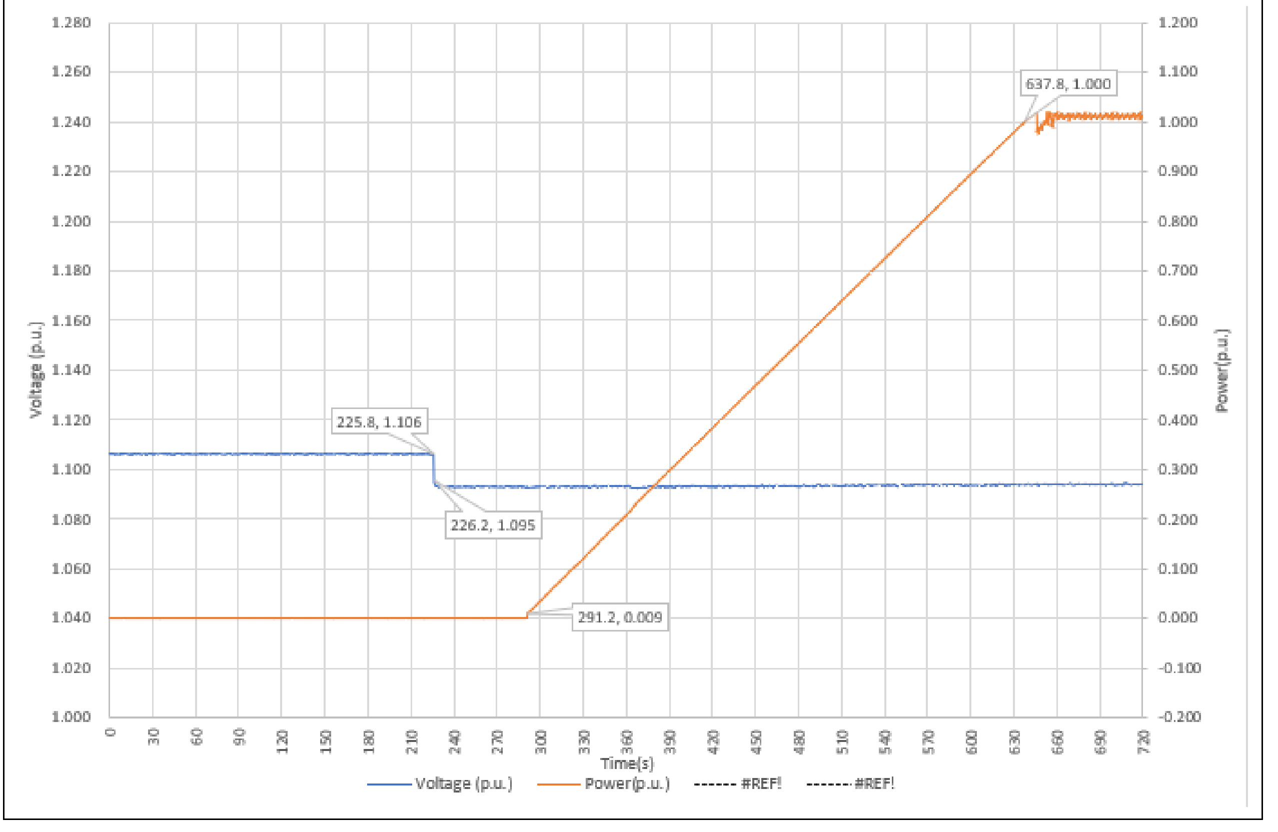


Over Voltage Connection





Voltage (p.u.)
Power(p.u.)
Time(s)
630.6, 1.000
218.4, 1.106
218.8, 1.096
284, 0.010
Voltage (p.u.)
Power(p.u.)
#REF!
#REF!



Voltage (p.u.)
Power(p.u.)
Time(s)
637.8, 1.000
225.8, 1.106
226.2, 1.095
291.2, 0.009
Voltage (p.u.)
Power(p.u.)
#REF!
#REF!

4.22.4 Voltage Reconnection

Test results are offered in the following tables:

Voltage Reconnection Value Limit	No Reconnection Test			Reconnection Test		
	Voltage value (%Un)	Time measured (s)	Reconnection	Voltage value (%Un)	Reconnection	Time measured (s)
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	63.2
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	63.6
V ≥ 94.0% Un	93.6%	>120	☒ NO ☐ YES	94.4%	☐ NO ☒ YES	64.2
V ≤ 110.0% Un	110.6%	>120	☒ NO ☐ YES	109.2%	☐ NO ☒ YES	64.2
V ≤ 110.0% Un	110.6%	>120	☒ NO ☐ YES	109.2%	☐ NO ☒ YES	63.4
V ≤ 110.0% Un	110.6%	>120	☒ NO ☐ YES	109.2%	☐ NO ☒ YES	63.4

The standard states that the tolerance limit for voltage reconnection values is ± 2 V, which is a 0,8% Un over 230 V, the reference voltage considered by the standard. So, 0.8% Un is the allowed tolerance to be considered for voltage reconnection value tests.

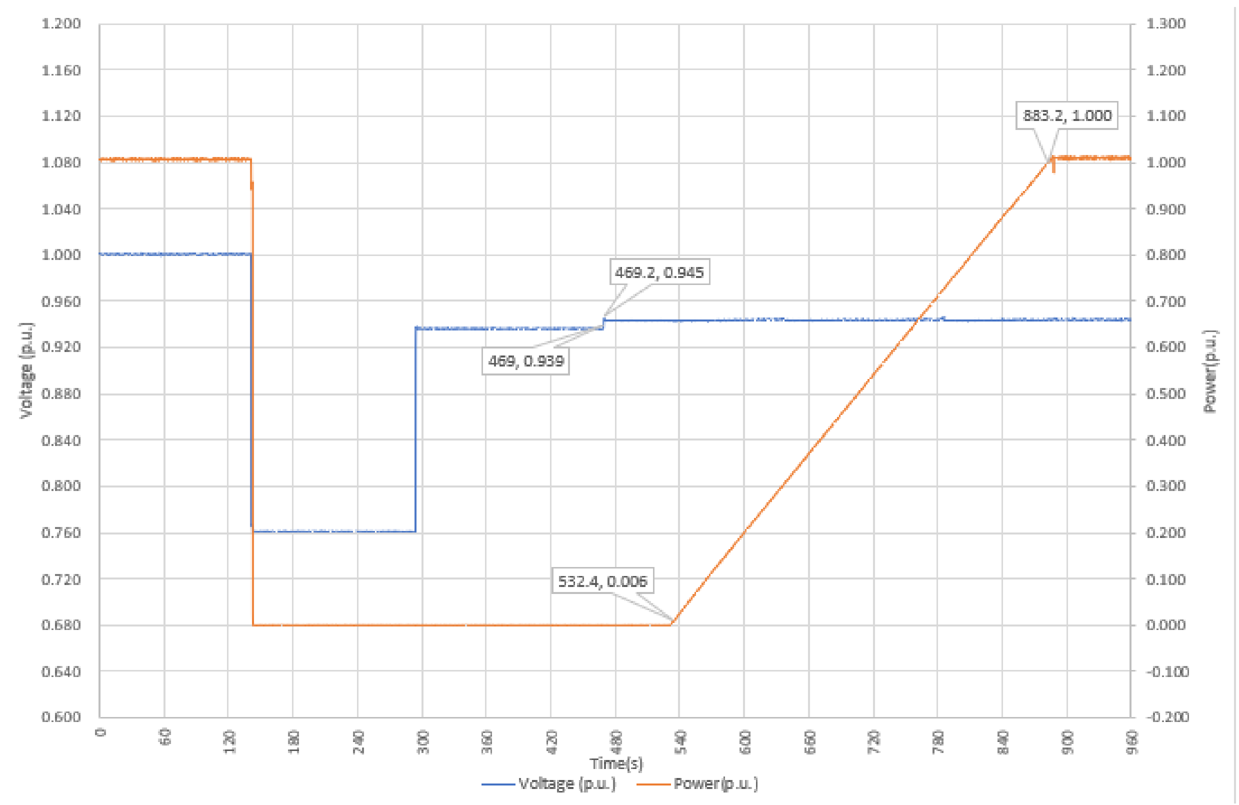
In addition to this requirement, it has been verified that according to the point 7.7 of the standard, the Control System of the inverter has a function to start reconnection following an adjustable Ramp Rate. The following table shows the programmed gradient for the different reconnections:

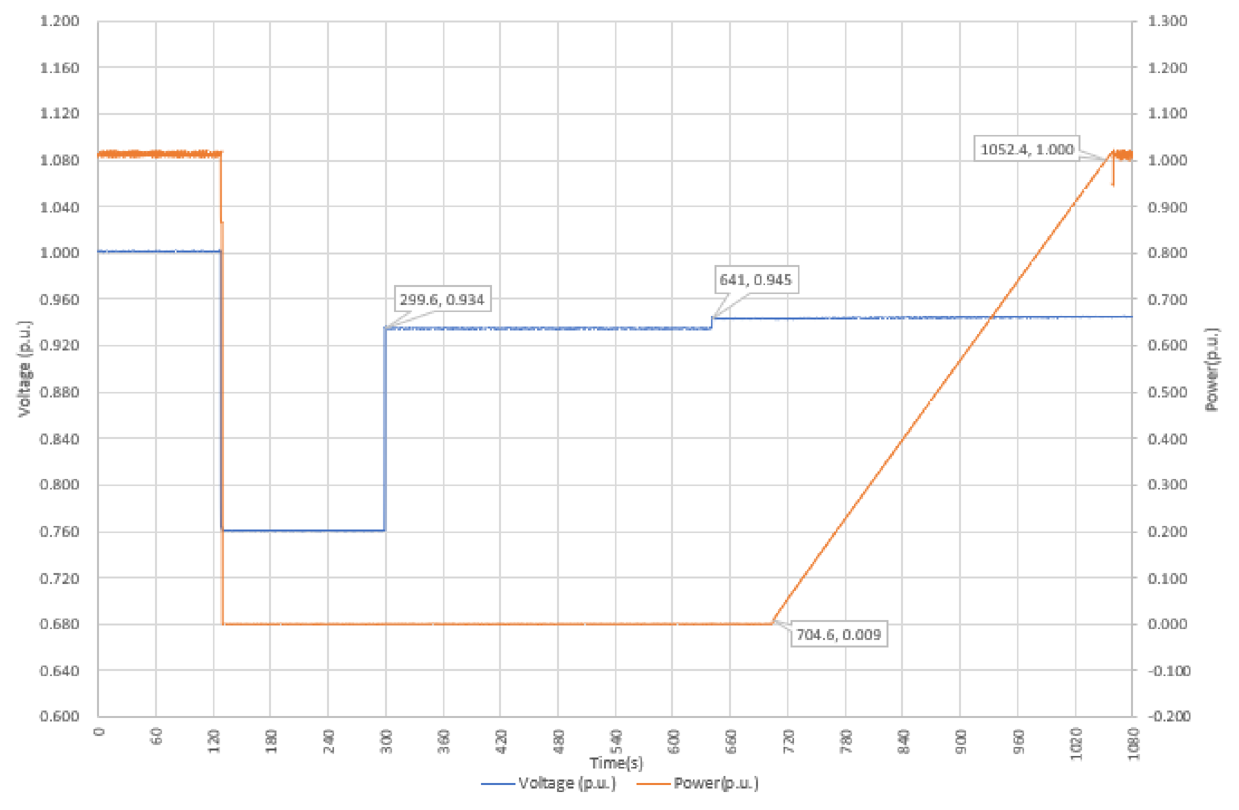
Voltage Reconnection Value Limit	Gradient (ΔP) desired (%P_n/min)	Gradient measured (P_n/min)
V ≥ 94.0% Un	≤ 100.0%	17.0%/17.3/17.3
V ≤ 110.0% Un	≤ 100.0%	17.0%/17.3/17.3

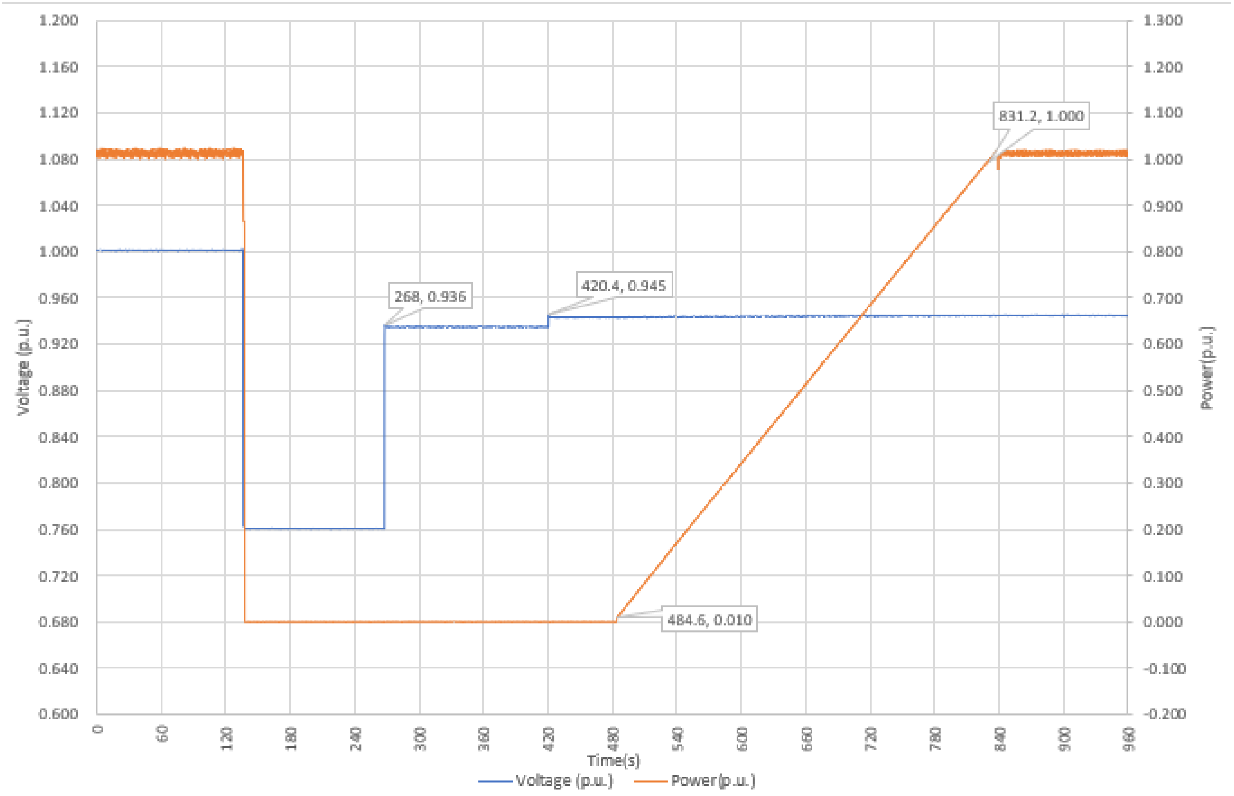
Note: it has been considered a minimum delay of 60 seconds to proceed with the start-up once the equipment is inside the required ranges.

Test results are graphically shown in following pages.

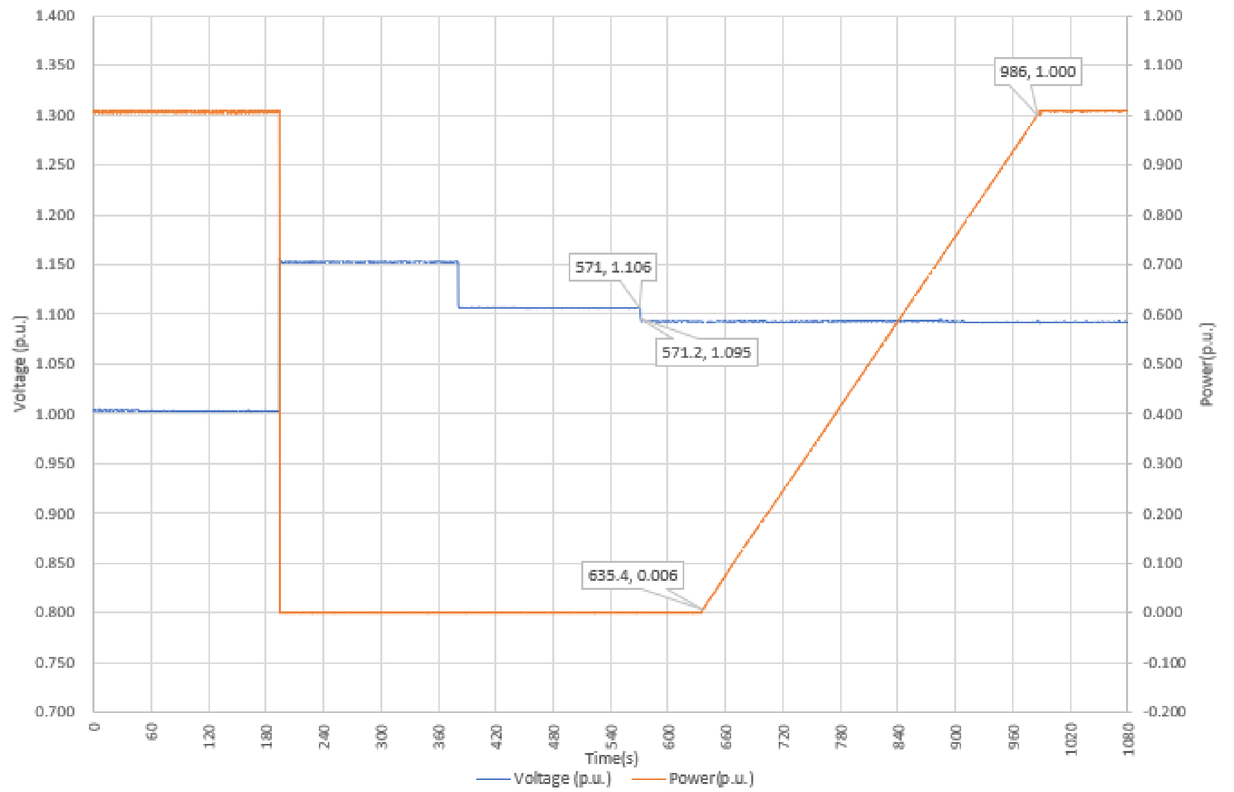
Under Voltage Reconnection

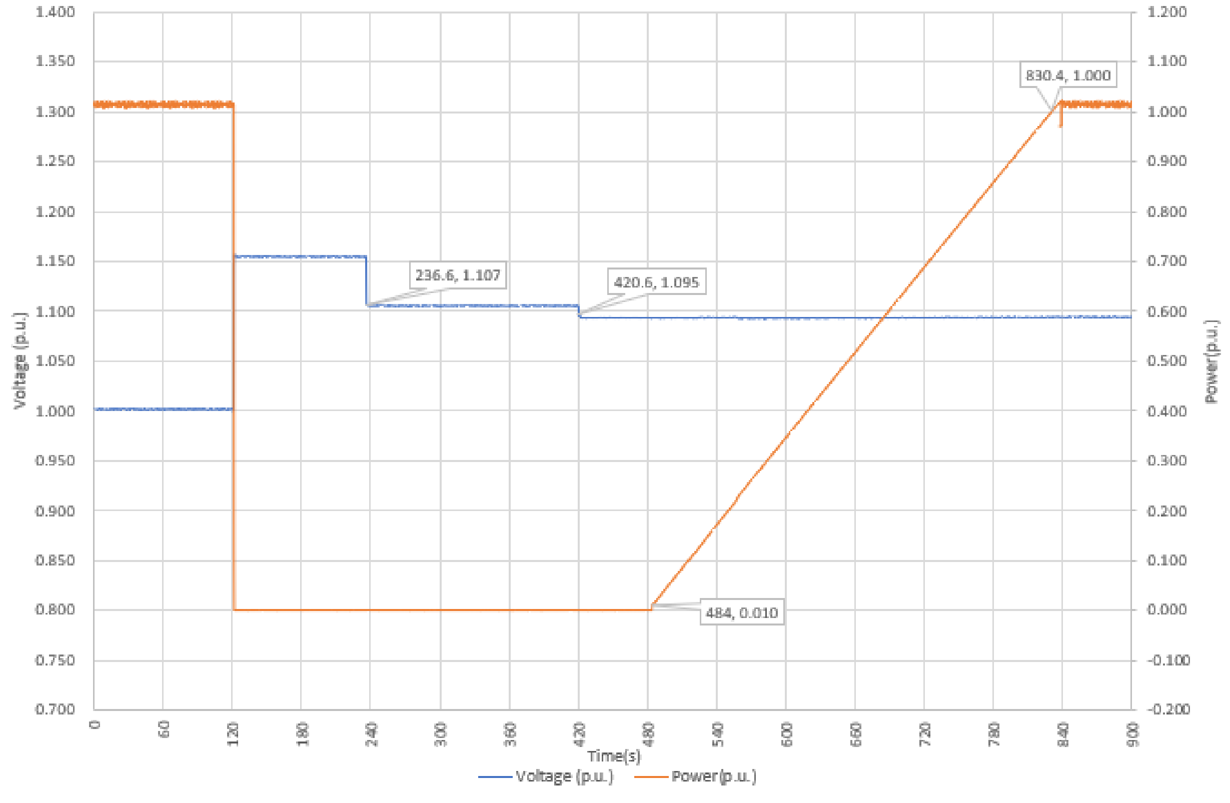




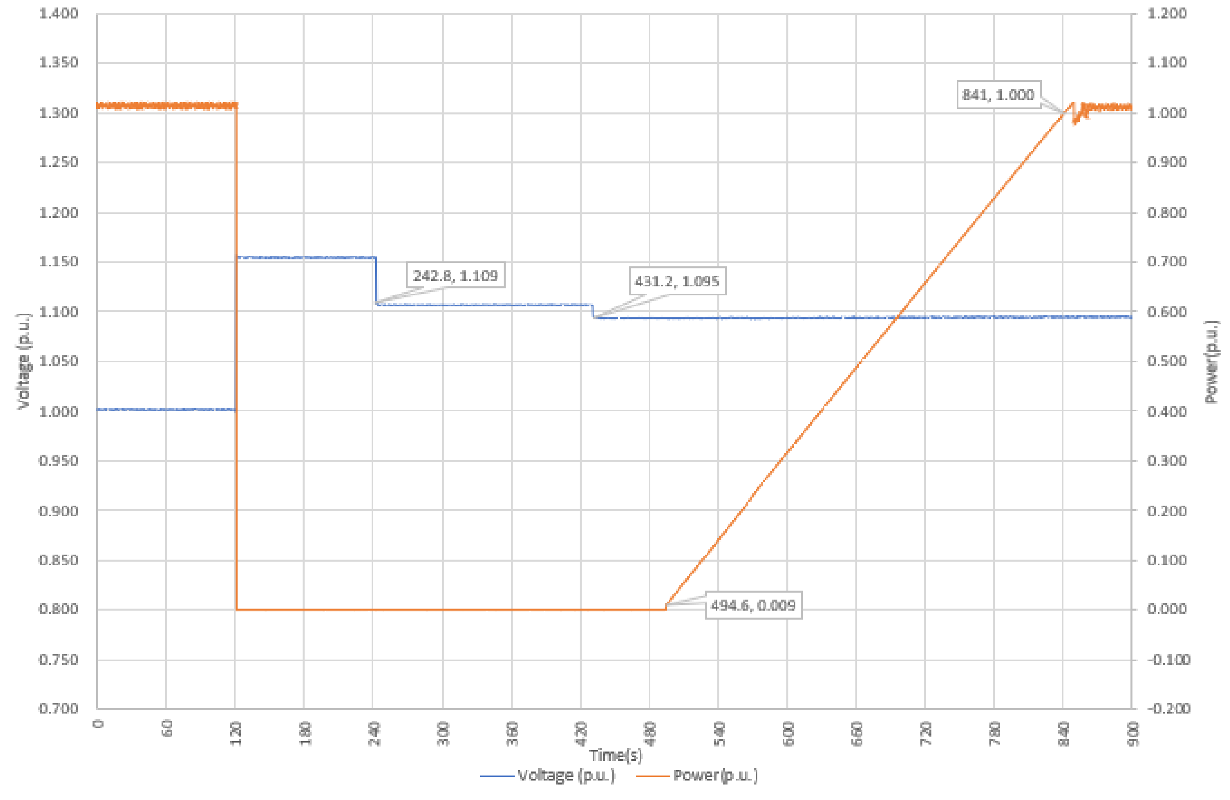


Over Voltage Reconnection





830.4, 1.000
236.6, 1.107
420.6, 1.095
484, 0.010
Voltage (p.u.)
Power(p.u.)
Time(s)



841, 1.000
242.8, 1.109
431.2, 1.095
494.6, 0.009
Voltage (p.u.)
Power(p.u.)
Time(s)

4.23 SECURITY OF PROTECTION SETTINGS

The inverter complies with the following requirements according to Clause 7.8 of the standard:

a) The inverter has been checked by inspection that changes to the internal setting shall require the use of a tool and special instructions not provided to unauthorized personnel.

b) The installer-accessible settings of the automatic disconnection device are capable of being adjusted within the limits specified in Clause 7.5 of the standard.

c) The manufacturer settings of the automatic disconnection device, specified in Clause 7.4 of the standard, are secured against changes.

4.24 MULTIPLE INVERTER COMBINATION

According to the clause 8 of the standard, Inverter energy systems are often comprised of multiple inverters used in combination to provide the desired inverter energy capacity or to ensure that voltage balance is maintained in multiple phase connections to the grid.

The inverter under testing doesn't have any of these functions incorporated in his control system, so this point is not applicable.

4.25 INVERTER MARKING AND DOCUMENTATION

The inverter is in compliance with marking and documentation requirements of IEC 62109-1, IEC 62109-2, and Clause 9 according AS/NZS 4777.2:2015

- IEC 62109-1 and IEC 62109-2: test report nº BL-DG2060127-B01 and BL-DG2060127-B01 attachment 1 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.
- IEC 62040-1: test report nº BL-DG2060127-B02 on 2020/07/02 which issued by Shenzhen BALUN Technology Co., Ltd.

According to points 9.2.4 and 9.2.5 the unit shall be marked with the following external or auxiliary systems if those are required to comply with the requirements from the standard:

External equipment requirement	Required (Yes or No?)
Isolation transformer	No
RCD / earth fault detection	No
External automatic disconnector (DRM0)	No
External device to enable extra DRM modes	No

AS/NZS 4777.2 : 2015			
Clause	Requirement - Test	Result - Remark	Verdict
9	INVERTER MARKING AND DOCUMENTATION		P
9.1	General		P
	The inverter shall comply with the marking and documentation requirements of IEC 62109-1 and IEC 62109-2, as varied by this Clause (9).		P
	All markings and documentation shall be in the English language.		P
9.2	Marking		P
9.2.1	General		P
	The following variations apply to the marking requirements of IEC 62109-1 and IEC 62109-2:		P
	(a) Inverters that are designated for use in inverter energy systems incorporating energy sources other than PV arrays or batteries shall bear additional or alternative markings appropriate to the energy source.		P
	(b) Inverters that are designated for use in closed electrical operating areas shall be marked with a warning stating that they are not suitable for installation in households or areas of a similar type or use (i.e. domestic).	Not used in closed electrical operationg areas.	N/A
9.2.2	Equipment ratings		P
	The inverter shall be marked with its ratings and the ratings of each port, as specified in Table 15. Only those ratings that are applicable to the type of inverter are required.		P

AS/NZS 4777.2 : 2015			
Clause	Requirement - Test	Result - Remark	Verdict
	The ratings shall be plainly and permanently marked on the inverter, in a location that is clearly visible after installation.		
9.2.3	Ports		P
	Each port shall be marked with its classification and indicate whether a.c or d.c. voltage as appropriate.		P
	Typical classifications include the following:		P
	(a) PV (photovoltaic).		P
	(b) Wind turbine.		N/A
	(c) Energy storage.		N/A
	(d) Battery.		P
	(e) Generator.		N/A
	(f) Grid-interactive.		P
	(g) Stand-alone.		P
	(h) Communications (type).		P
	(i) DRM.		P
	(j) Load.		P
9.2.4	External and ancillary equipment		N/A
	If the inverter requires external or ancillary equipment for compliance with this Standard, the requirement for any such equipment shall be marked on the inverter along with the following or an equivalent statement: 'Refer to the installation instructions for type and ratings' or symbol.		N/A
	Any external or ancillary equipment shall be marked in accordance with this Clause (9).		N/A
9.2.5	Residual current devices (RCDs)		P
	Inverter energy systems used with PV array systems require residual current detection in accordance with IEC 62109-1 and IEC 62109-2. The requirements can be met by the installation of a suitably rated RCD external to the inverter or by an RCMU integral to the inverter.	An RCMU integral to the inverter used	P
	Where an external RCD is required, the inverter shall be marked with a warning along with the rating and type of RCD required. The warning shall be located in a prominent position and written in lettering at least 5 mm high. It shall contain the following or an equivalent statement:		N/A
	WARNING: AN RCD IS REQUIRED ON THE [NAME] PORTS OF THE INVERTER		N/A

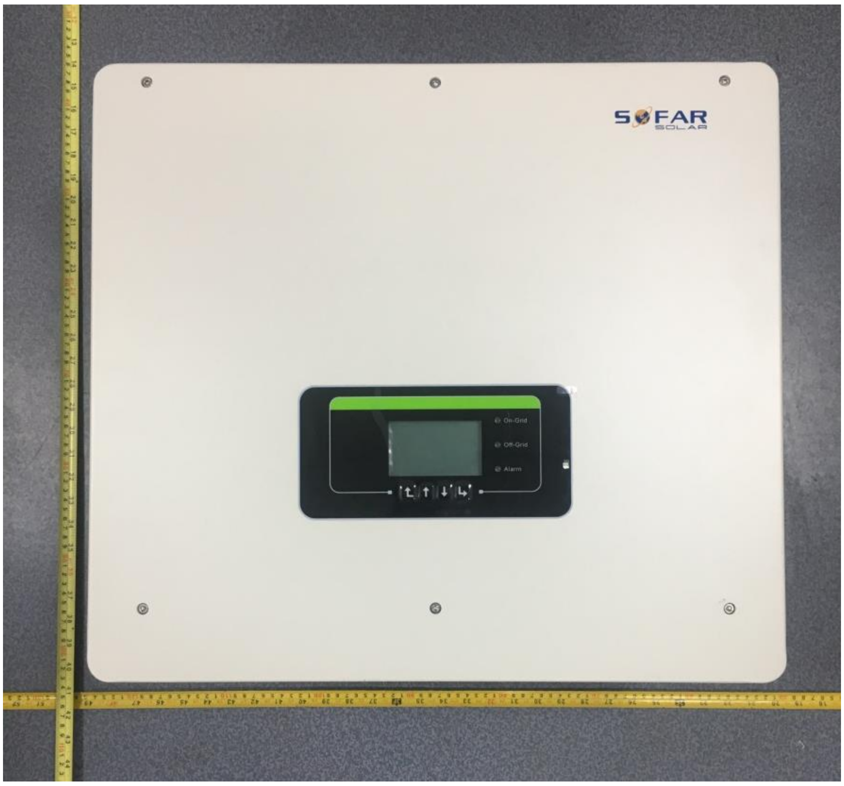
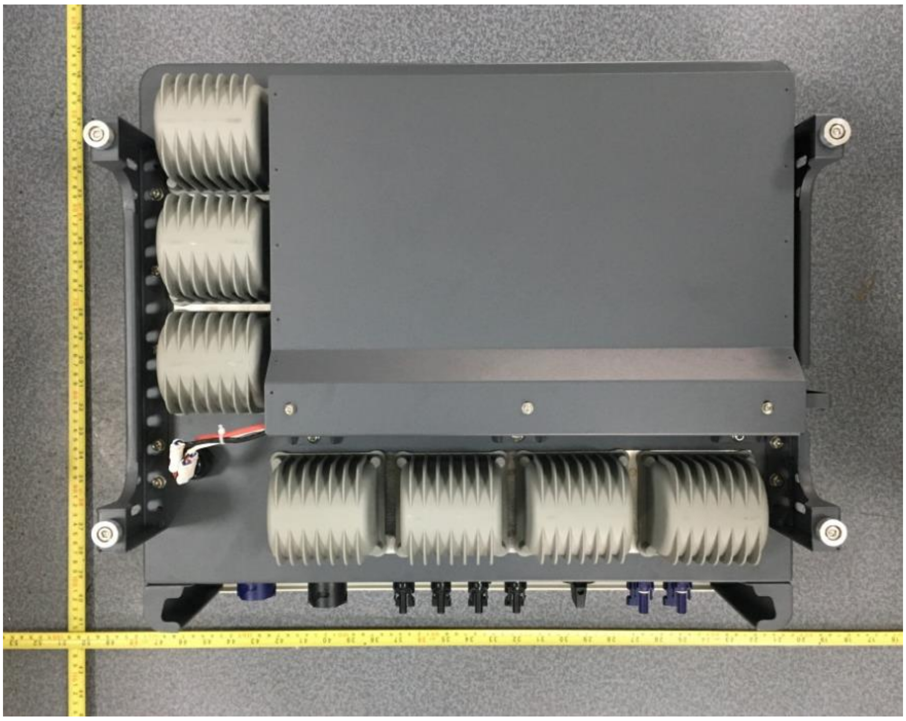
AS/NZS 4777.2 : 2015			
Clause	Requirement - Test	Result - Remark	Verdict
	If the inverter energy system requires a Type B RCD, the inverter shall be marked with a warning. The warning shall be located in a prominent position and written in lettering at least 5 mm high. It shall contain the following:		N/A
	WARNING: A TYPE B RCD IS REQUIRED ON THE [NAME] PORTS OF THE INVERTER		N/A
9.2.6	Demand response modes		P
	The demand response modes supported by the inverter should be permanently marked on the name plate or on a durable sticker located on or near the demand response interface port to indicate the demand response modes of which the unit is capable.	DRM 0, DRM1-8	P
	Figure 9 illustrates an acceptable form of marking. If this form of marking is used, each box shall contain a tick or a cross (if the inverter has that capability) or remain blank (if it does not have that capability). Alternatively, only the modes supported may be marked.		P
	If the physical interface is a terminal block, then—	Terminal block used	P
	(a) the terminals shall be engraved or otherwise durably marked; or		P
	(b) a permanent label with ‘DRM Port’ shall be affixed near the terminal block.		P
	The marking shall indicate which terminal corresponds to which demand response mode.		P
	The range of markings is indicated against Pins 1 to 6 in Table 7.		P
9.3	Documentation		P
9.3.1	General		P
	The documentation supplied with the inverter shall provide all information necessary for the correct installation, operation and use of the system and any required external devices including information specified in Clause 9.2.		P
	All inverters, including those intended for use in systems incorporating energy sources other than PV arrays or batteries, shall comply with the documentation requirements of IEC 62109-1 and IEC 62109-2.		P
9.3.2	Equipment ratings		P
	The documentation supplied with the inverter shall state the ratings of the inverter and the ratings for each port, as specified in Table 16. Only those ratings that are applicable to the type of inverter are required.		P

AS/NZS 4777.2 : 2015			
Clause	Requirement - Test	Result - Remark	Verdict
	For equipment with rated current greater than 16 A per phase, additional documentation requirements apply. See Clause 5.7.		P
9.3.3	Ports		P
	In addition to the requirements of Clause 9.3.2, the documentation supplied with the inverter shall state the following for each port, as a minimum:		P
	(a) Means of connection.		P
	(b) For pluggable equipment type B, the type of matching connectors to be used.		P
	(c) External controls and protection requirements.		P
	(d) Explanation of terminals or pins used for connection including polarity and voltage.		P
	(e) Tightening torque to be applied to terminals.		N/A
	(f) Instructions for protective earthing.		P
	(g) Instructions for connection of loads and installation of RCD protection to stand-alone ports.		N/A
	(h) The decisive voltage class (DVC).		P
9.3.4	External and ancillary equipment		N/A
	Where an inverter or multiple inverter combinations requires external or ancillary equipment for compliance with this Standard, the documentation shall—		N/A
	(a) state the requirement for any such equipment;		N/A
	(b) provide sufficient information to identify the external or ancillary equipment, either by manufacturer and part number or by type and rating; and		N/A
	(c) specify assembly, location, mounting and connection requirements.		N/A
9.3.5	RCDs		N/A
	Where an external RCD is required, the following or an equivalent statement shall be included in the documentation: ‘External RCD Required’. The documentation shall also state the rating and type of RCD required and provide instructions for the installation of the RCD.	An RCMU integral to the inverter used	N/A
9.3.6	Multiple mode inverters	Grid-connected mode or standalone mode	P

AS/NZS 4777.2 : 2015			
Clause	Requirement - Test	Result - Remark	Verdict
	Where the inverter is capable of multiple mode operation, the documentation shall include the following:		P
	(a) Ratings and means of connection to each source of supply to the inverter or output from the inverter.		P
	(b) Any requirements related to wiring and external controls, including the method of maintaining neutral continuity within the electrical installation to any stand-alone ports as required.		P
	(c) Disconnection means and isolation means.		N/A
	(d) Overcurrent protection needed.		N/A
9.3.7	Multiple inverter combinations	No in such used	N/A
	Where an inverter has been tested for use in a multiple inverter combination as per Clause 8, the documentation shall include the following:		N/A
	(a) Valid combinations of inverters.		N/A
	(b) Installation instructions for correct operation as a multiple inverter combination.		N/A

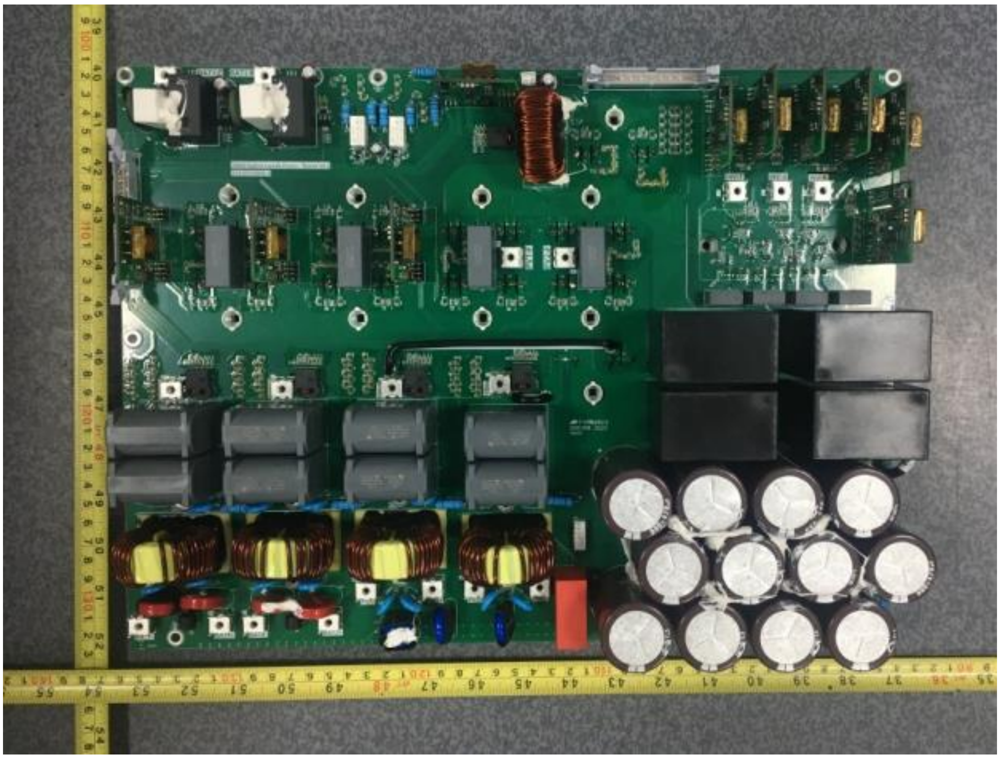
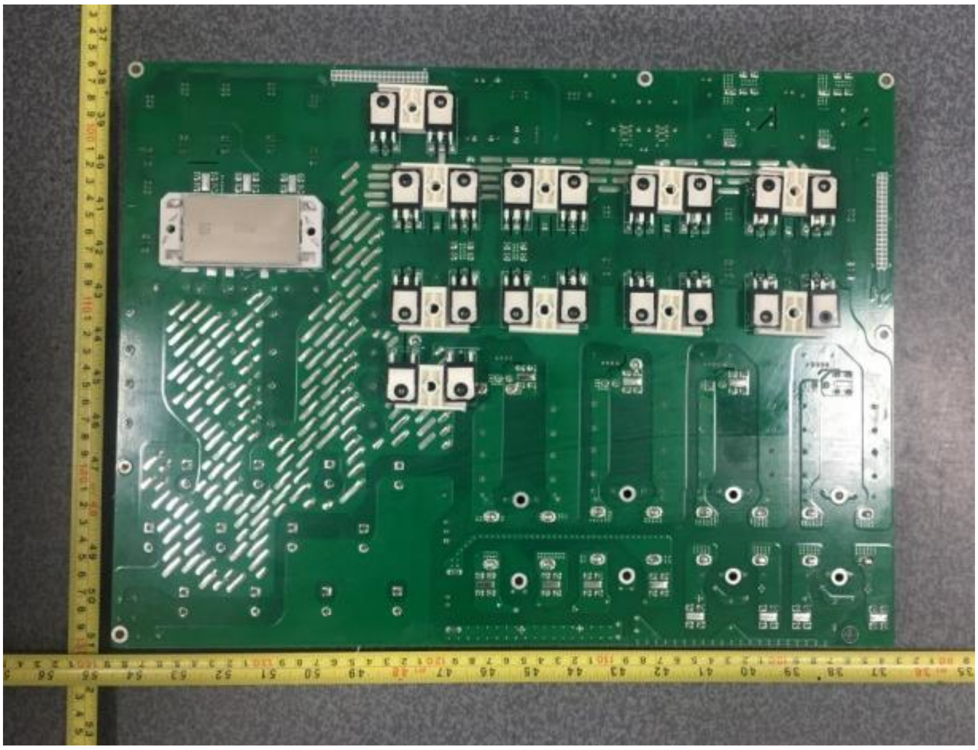
5 PICTURES

Refer to the pictures below for details.

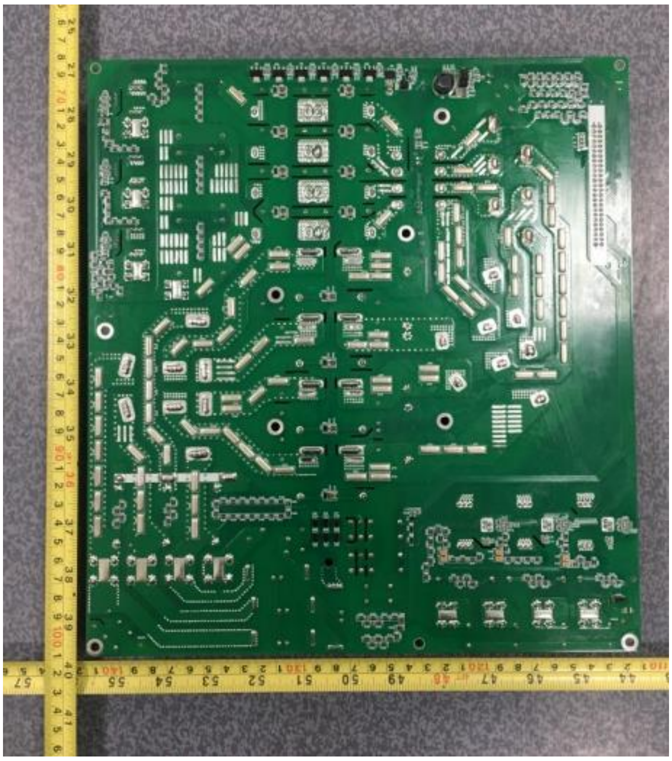
Front View

Back View


Side View

Connectors

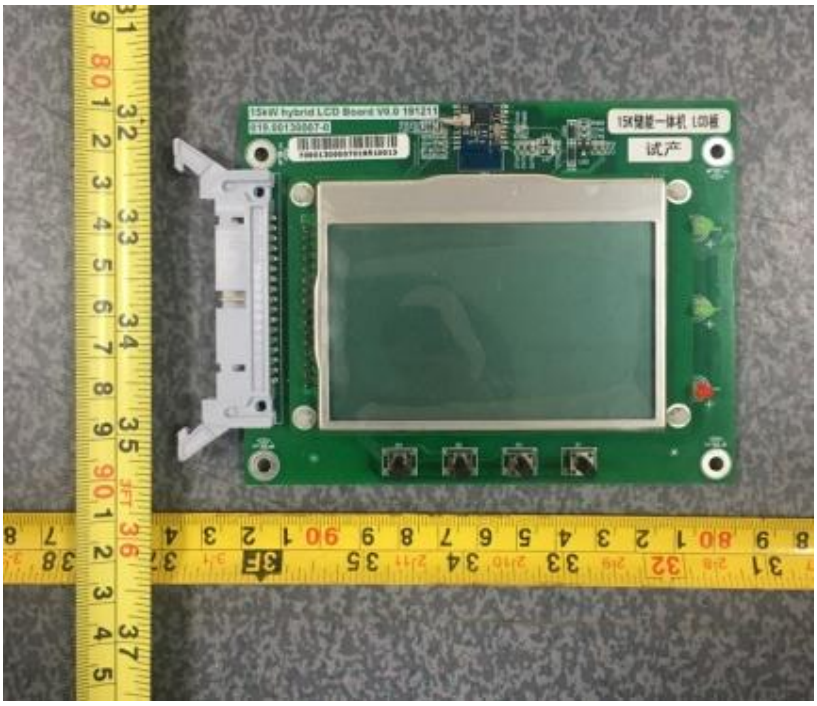
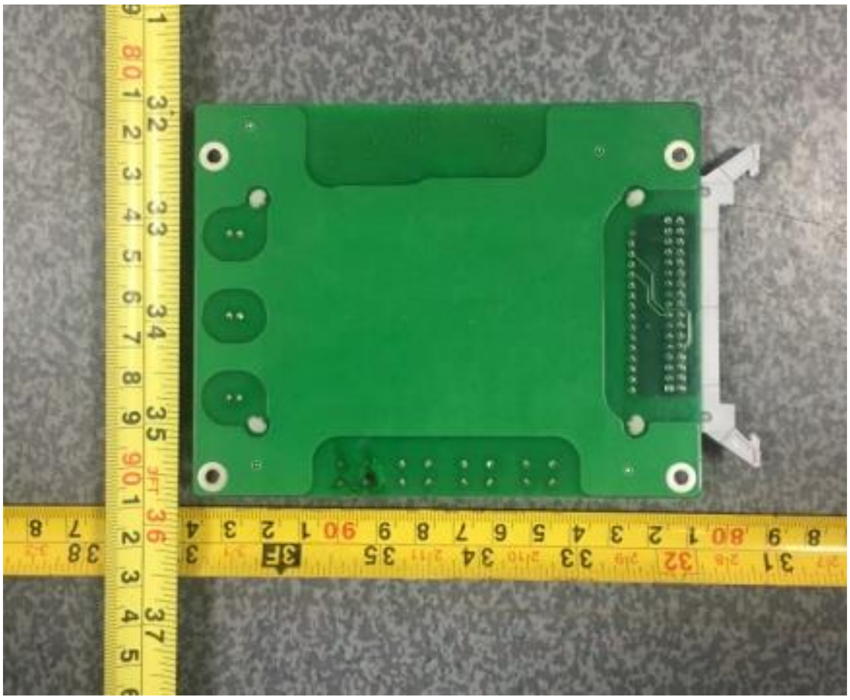
Front View of Power Board

Back View of Power Board


Front View of Output Board

Back View of Output Board


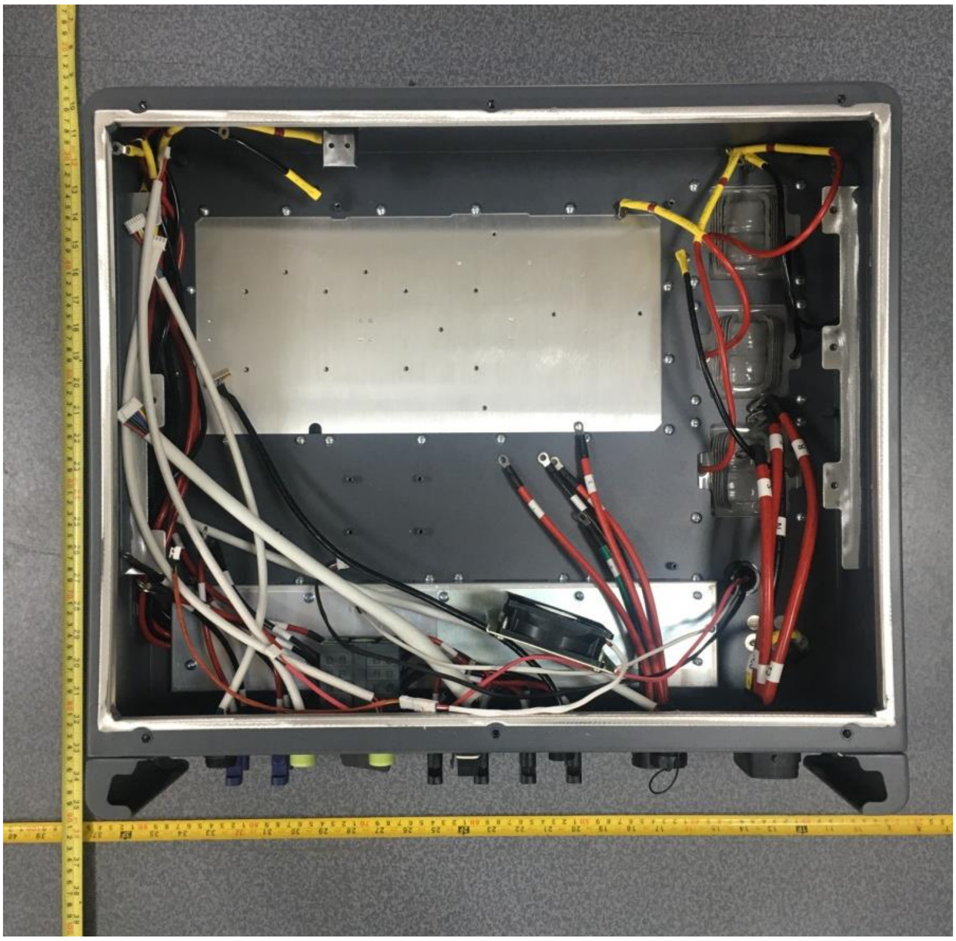
Front View of Control Board

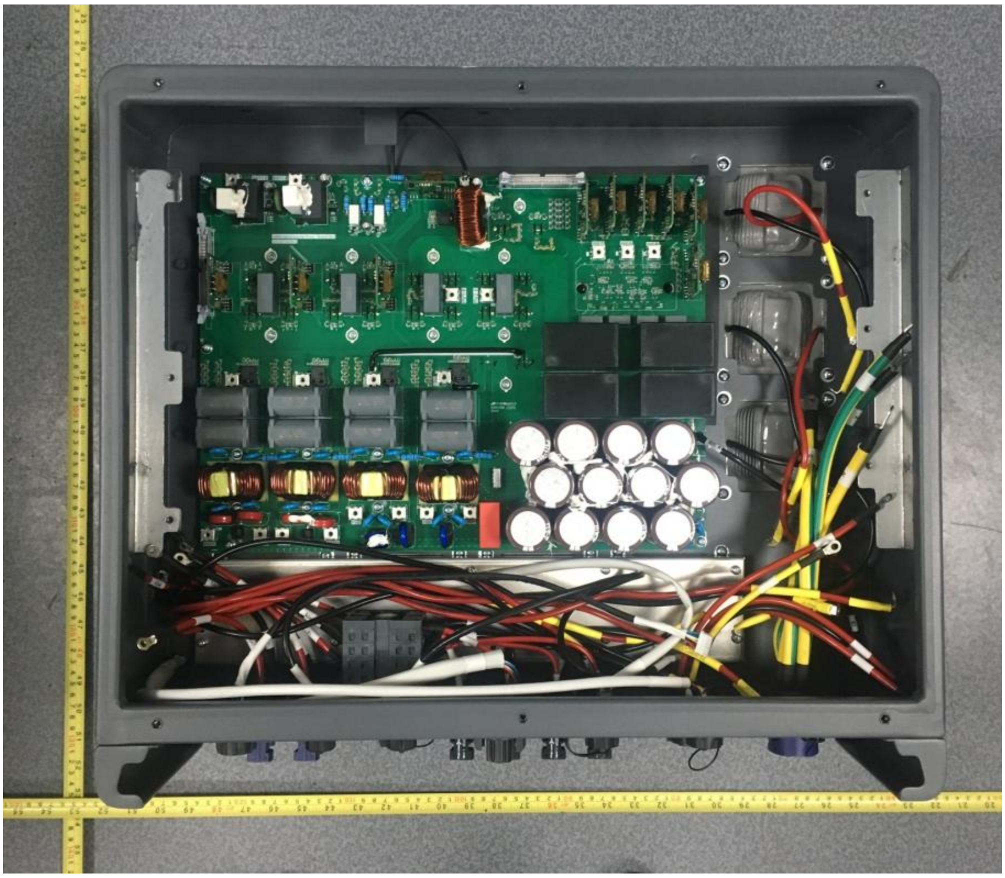
Back View of Control Board


Front view of Display Screen

Back view of Display Screen


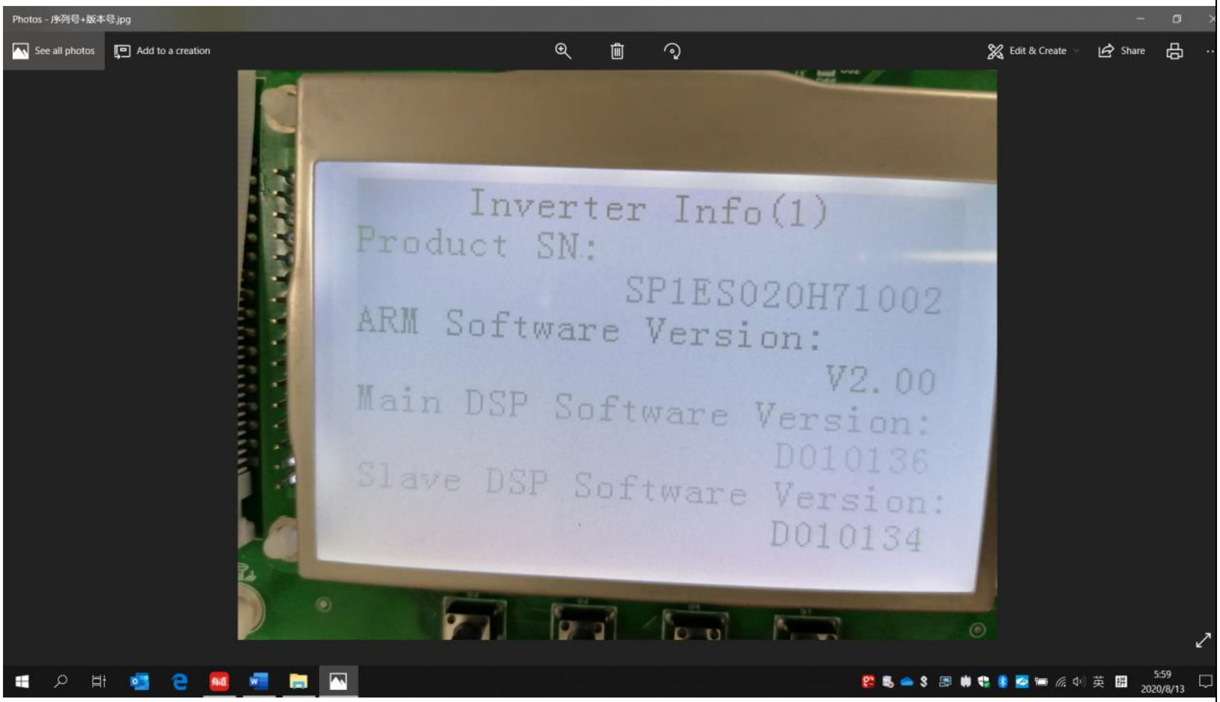
Ground Wire

Internal of the Casing



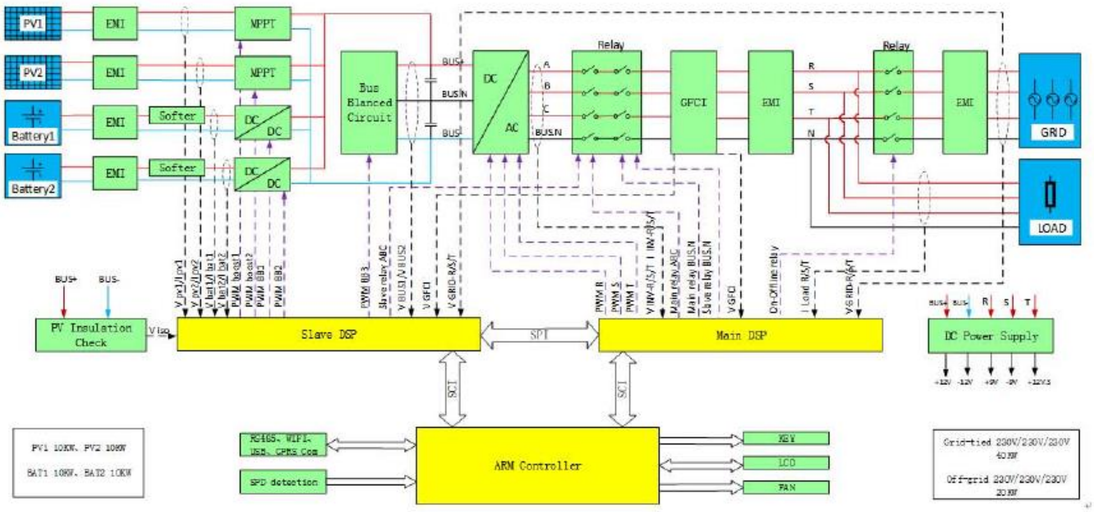
Devices of Back Layer

Devices of Front Layer


Sofeware Version



6 ELECTRICAL SCHEMES

Equipment under testing



---END OF REPORT---